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TiO_2 as intermediate buffer layer in $Cu(In,Ga)Se_2$ solar cells

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ABSTRACT

The application of TiO_2 as part of the buffer layer stack in thin film $Cu(In,Ga)Se_2$ (CIGS) solar cells is investigated for the improvement of the photovoltaic device performance. In a standard device configuration a CdS/ZnO/Al:ZnO layer stack is applied onto the CIGS absorber layer. By decreasing the CdS buffer layer thickness a higher photocurrent is expected from a reduced parasitic absorption. When the CdS layer is not fully covering the CIGS surface, losses in V_{OC} and FF are observed in I-V measurements due to the arising unfavorable CIGS/ZnO band alignment and sputter damage on the CIGS surface. Here we present thin TiO_2 layers deposited by atomic layer deposition at low temperature as alternative to the unintentionally doped ZnO. With this approach, the photocurrent can be increased without adversely affecting V_{OC}. Comparable device efficiency is achieved for the investigated structure and the reference process with the gain in current density being compensated by increased series resistance. Temperature dependent I-V measurements coupled with 1D-SCAPS simulations suggest a positive conduction band offset at the CdS/TiO_2 interface limiting the FF. ALD-TiO_2 is suggested as a more suitable intermediate buffer layer than sputtered ZnO when thin CdS buffer layers are applied.

1. Introduction

Solar cells based on chalcopyrite $Cu(In,Ga)Se_2$ (CIGS) absorbers are among the most promising thin-film photovoltaic technologies with laboratory scale power conversion efficiencies (PCE) reaching 20.4% on a flexible polymer substrate [1] and 22.6% on a soda lime glass (SLG) substrate [2]. CdS grown by chemical bath deposition (CBD) is commonly employed as a buffer layer in CIGS solar cells enabling the aforementioned champion device efficiencies. The relatively low band-gap energy of CdS (2.4–2.5 eV), however, limits the optimum performance of the cells due to parasitic absorption in the short wavelength region [3].

In order to reduce this parasitic absorption several approaches have been proposed by applying alternative buffer layers with a wider bandgap and/or lower absorption coefficient such as Zn(S,O,OH), $Zn_{1-x}Sn_xO_y$, In_xS_y and $Zn_xMg_{1-x}O$ achieving a PCE of 21.0% [4], 18.2% [5], 18.2% [6] and 18.1% [7], respectively. Amorphous TiO_2 has also been reported to work as a buffer layer on a non-vacuum deposited CIGS absorber but with limited PCE of 9.9% for a cell with active area of 10.5 mm^2 [8].

Another approach to minimize the optical losses is the reduction of the CdS layer thickness. It has been reported that a minimal thickness of about 50 nm is necessary for optimal performance in CIGS cells without an alkaline post deposition treatment (PDT) [9,10]. The application of KF PDT allowed for a reduction of the CdS thickness down to about 30 nm [1]. A further thickness reduction, however, leads to a non-uniform coverage of the CIGS surface and severe degradation of the current-voltage (I-V) parameters V_{OC} and FF [11]. This is supposed to stem from a cliff-like band alignment and thus carrier recombination at the CIGS/ZnO interface [12–14] and sputter damage on the CIGS surface from the subsequent ZnO/Al:ZnO window layer deposition [14–16]. The application of a thin Al_2O_3 layer deposited by atomic layer deposition (ALD) on top of CBD-CdS was reported to partially mitigate the losses in V_{OC} and FF for CdS layers thinner than 30 nm. The thickness constraint to about 1 nm of the highly resistive Al_2O_3, however, sets a limit to the achievable V_{OC} recovery [11].

A different approach was taken by Kobayashi et al. [15] by successfully replacing the sputtered Al:ZnO window layer with B:ZnO deposited by metal-organic chemical vapor deposition (MOCVD) when a thin (10 nm) Zn(S,O,OH) buffer layer was used. The work of Minemoto and Julayhi focused on optimizing the band-alignment with a sputtered $Al:ZnO_{1-x}S_x$ window layer in a buffer-less CIGS cell concluding that the inferior conversion efficiency is due to sputter damage on the CIGS surface [16]. What is not considered with this approach are further beneficial effects of a buffer layer: e.g. a possible buried junction, positioning of the interface Fermi level close to the absorber conduction band and surface inversion, mitigating harmful defects (see [3,17]).

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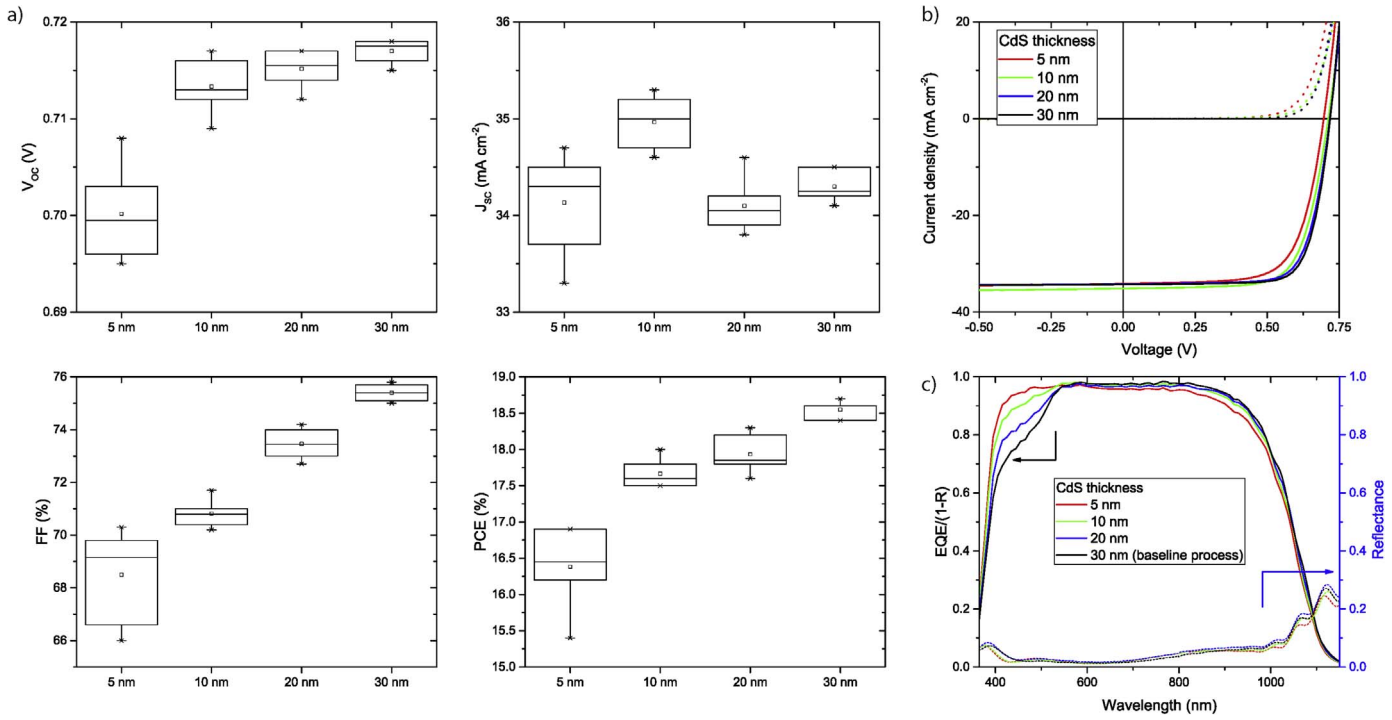

Fig. 1. a) Boxplot chart (6 best performing cells of each sample) of the current-voltage parameters of a baseline structure SLG/Mo/CIGS/CdS/ZnO/Al:ZnO/grid(Ni,Al)/MgF_2 with varying CdS buffer layer thickness from ~ 5–30 nm. b,c) corresponding J-V curves, internal quantum efficiency and reflectance measurement of representative cells.

In this contribution a thin CdS layer is combined with an ALD-TiO_2 to constitute the interlayer structure between the CIGS absorber and Al:ZnO front contact. With this approach the CIGS/CdS interface and band-alignment is maintained while the CIGS/ZnO interface is avoided in case of insufficient CdS coverage. Furthermore TiO_2 is replacing ZnO as highly transparent and resistive (HTR) layer in its function of preventing electrical inhomogeneities and shunt paths [18,19]. The soft deposition method thermal-ALD is selected to mitigate sputtering damage on the CIGS surface and for a precise thickness control of the deposited TiO_2.

2. Experimental section

2.1. Sample fabrication

The architecture of the multilayer device under investigation is SLG/SiO_2/Mo/CIGS/CdS/HTR/Al:ZnO/MgF_2 where the baseline unintentionally doped ZnO HTR layer is replaced with TiO_2.

The CIGS absorber layers were deposited on SiO_2 and Mo coated soda lime glass (SLG) substrates by elemental co-evaporation from effusion cells at a base pressure of ~ 10^{-5} Pa in a multi-stage process as reported before [20]. Additionally a NaF and RbF PDT was performed. The absorber layer composition was measured by x-ray fluorescence giving a [Cu]/([In] + [Ga]) ratio of 0.83–0.86 and a [Ga]/([Ga] + [In]) ratio of 0.44–0.46. An absorber layer thickness of 3 µm was determined by scanning electron microscopy (SEM).

The CdS buffer layer was deposited by CBD from a bath of cadmium acetate (2.1 mM), thiourea (22 mM) and ammonium hydroxide (2 M [NH_3]) at 70 °C. The thickness was controlled by the time the sample was immersed in the bath. After the deposition a short annealing (2 min) at 180 °C and ambient atmosphere was performed. The thickness of CdS was determined by SEM for layers with a thickness above 20 nm. For thinner layers the thickness was estimated by reproducing the CdS absorption in the blue region of the EQE measurements using as input the extinction coefficient of CdS.

For the reference structure ~ 60 nm ZnO was deposited by rf-magnetron sputtering in an Ar/O_2 (0.02%) atmosphere at a pressure of 0.46 Pa and a power density of 1.9 W cm^{-2}. The alternative HTR layer TiO_2 was deposited by ALD at a substrate temperature of 100 °C from tetrakis(dimethylamino)titanium(IV) (TDMAT) and H_2O with a Fiji G2 system (Ultratech). Ar was used as carrier gas at a base pressure of 28 Pa. The source temperature of TDMAT was at 75 °C while H_2O was kept at room temperature. A saturated growth of 53 ± 0.2 pm/cycle was determined by ellipsometry on Si (100) reference substrates for the ALD cycle of H_2O/Ar purge/TDMAT/Ar purge using pulse lengths of 0.06/65/0.6/65 s, respectively. SEM micrographs of TiO_2 on CIGS or on CIGS/CdS showed a comparable growth rate with a larger uncertainty. No post deposition annealing was performed on the TiO_2 layer which is therefore assumed to be amorphous as reported for comparable deposition conditions [21–23].

The cells were finished with a sputtered ~ 260 nm Al:ZnO (2%$_{at}$ Al, 1.8 W cm^{-2}), 105 nm of MgF_2 and 4 µm Ni/Al grid by e-beam evaporation. Mechanical scribing was used to define a cell area of 0.25 ± 0.02 cm^2.

2.2. Characterization methods

I-V curves were measured with a Keithley 2400 source meter and four-terminal sensing under standard test conditions (1000 W m^{-2}, 298 K) using a type ABA solar simulator. Temperature dependent measurements were performed in a cryostat with liquid nitrogen cooling and a halogen lamp. External quantum efficiency (EQE) measurements were performed with a chopped white light source (halogen), a tripple-grating monochromator and a lock-in amplifier under ~ 100 W m^{-2} white light bias at 298 K. A monocrystalline Si solar cell certified by Fraunhofer ISE was used as a reference. The internal quantum efficiency (IQE) was calculated with EQE/(1-R) where R denotes the reflectance. Reflectance measurements were performed on a Shimadzu UV-3600 spectrophotometer. SEM was performed on a Hitachi S-4800 electron microscope.

3. Results and discussion

The effect of reducing the CdS buffer layer thickness on the cell

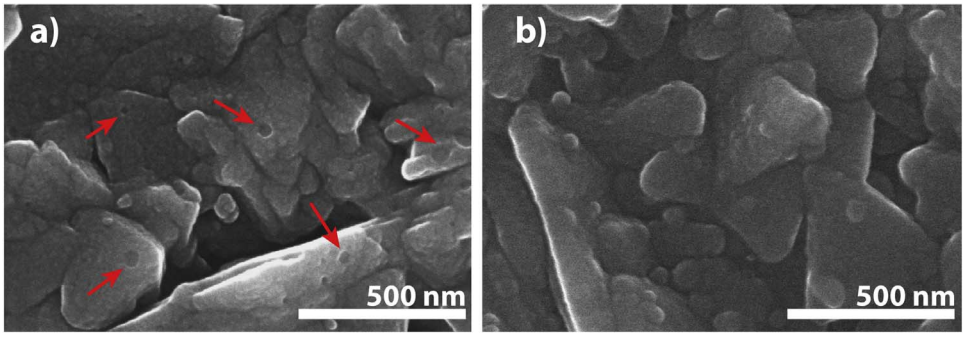

Fig. 2. SEM top-view micrograph of the CdS buffer layer after 10 (a) and 16 (b) minutes deposition on top of the CIGS absorber. No conductive coating was applied. Numerous pinholes in the CdS layer in case a) are visible.

performance is quantified for the baseline configuration with the standard unintentionally doped ZnO HTR layer. Fig. 1 depicts the IQE and current-voltage characteristics of these cells. The CdS layer thickness was adjusted by reducing the length of the chemical bath from 16 min (standard deposition time) to 13, 10 and 7 min. This leads to a CdS thickness of about 30, 20, 10 and 5 nm, respectively. The IQE clearly shows the parasitic absorption losses in the blue wavelength region (~ 380–550 nm) that scale with the CdS thickness. A reduced response in the near infrared region is observed for cells with a thin CdS buffer layer. Hence the gain in current caused by less parasitic absorption in cells with reduced CdS layer thickness is only partially reflected in the corresponding I-V measurements. For the thinnest layer the largest loss in V_{OC} and FF is observed. The overall trend is similar to what has been reported [9,11]. Fig. 2 shows top-view SEM micrographs of ~ 10 nm (Fig. 2a) and ~ 30 nm (Fig. 2b) CdS on the CIGS surface. In the former case the CIGS surface is not fully covered and pinholes in the CdS layer up to ~ 40 nm in diameter are present.

Therefore, in the following a new device structure is tested: the CdS layer thickness is reduced and TiO_2 is used as HTR layer substituting the unintentionally doped ZnO. Fig. 3b shows an SEM micrograph of the investigated structure compared to the baseline reference (Fig. 3a). The TiO_2 layer is deposited by ALD, which allows for a plasma-free, homogeneous growth and precise thickness control. The aim of the ALD-TiO_2 is a reduction of the effect of shunt paths and sputter damage on the absorber layer. Effects of plasma damage are discussed in the Supporting information (S1). To reduce the thermal budget a relatively low deposition temperature of 100 °C was chosen. At this temperature no detrimental effect on the SLG/SiO_2/Mo/CIGS/CdS is expected. This observation was verified by thermal treatment under the same conditions and for comparable time as during a typical ALD process of reference devices.

Fig. 4 shows the PV parameters of CIGS solar cells with ALD-TiO_2 as HTR layer and different CdS buffer layer thicknesses. The CIGS absorbers from the same CIGS deposition run were immersed for four different times (7, 10, 13, 16 min) into the solution for the CBD-CdS resulting in a thickness variation of the CdS layer of 5, 10, 20 and 30 nm on which then 15 nm TiO_2 were deposited. A trend with buffer layer thickness for all PV parameters is observed: The V_{OC} decreases by a similar percentage as the current density (see also EQE) increases (about 2–3%) when reducing the CdS thickness from 30 to 5 nm. This trend is comparable to what has been observed in the study with unintentionally doped ZnO as HTR layer (compare to Fig. 1b). However, the losses in FF are much less severe with about 4% (TiO_2, Fig. 4) compared to 9% (ZnO, Fig. 1b) when reducing the CdS thickness. Hence the PCE is less influenced by the buffer layer thickness when using TiO_2 as HTR layer. The highest average efficiency is obtained with the ~ 10 nm CdS (10 min CBD) layer. Therefore subsequent experiments are based on a 10 nm CdS layer.

The effect of different ALD-TiO_2 layer thickness but fixed CdS buffer layer thickness is illustrated in Fig. 5. An optimum for the PCE is found at about 15 nm of TiO_2 thickness with all PV parameters following the same trend. The samples comprising thinner layers, i.e. 2 and 5 nm TiO_2, are similar in their performance with all PV parameters inferior to the 15 nm TiO_2 sample. The IQE of the cells is comparable, although the reflectance in the cell comprising the thin TiO_2 is slightly higher and the integrated current density is lower. For a thick TiO_2 layer (20 nm) a much reduced FF is observed, a similar trend to what has been reported on the thickness dependency of the FF when unintentionally doped ZnO is used as HTR layer [19]. A comparison of different buffer layer configurations is shown in Fig. 6. When no HTR layer is applied, the lowest overall solar cell performance is obtained. A 15 nm thick TiO_2 HTR layer outperforms ZnO when a thin CdS buffer layer is used in all parameters and yields a PCE equal to a reference structure comprising a thick CdS and ZnO buffer layer stack. The average gain in current density compared to this reference is about 0.7–0.8 mA cm^{-2} as determined from I-V and EQE measurements (compare IQE in Fig. 6c). The FF, however, is inferior.

A reduced FF ("roll over" behavior, i.e. the I-V curve shows a current saturation in forward bias [24]) was reported when Al_2O_3 was applied as passivation layer at the CdS/ZnO interface [11] or when TiO_2 was used as buffer layer in CIGS solar cells [8]. Based on these observations, the discussion about a larger positive conduction band offset for a CIS/TiO_2 than a CIS/CdS interface in [8] and simulations on the buffer/HTR layer band alignment in [25] it is suggested that the herein applied TiO_2 HTR layer may introduce a positive conduction band offset at the buffer/window interface.

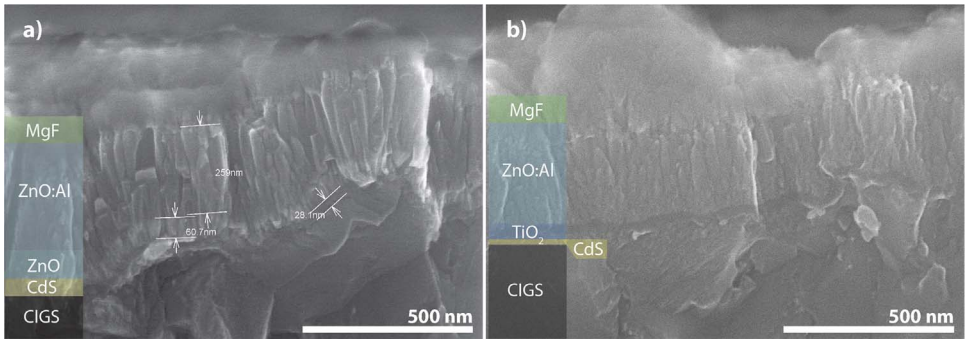

Fig. 3. SEM cross-sectional micrograph of a) CIGS/CdS(~30 nm)/ZnO(~60 nm)/Al:ZnO/MgF_2 and b) CIGS/CdS (~10 nm)/TiO_2(20 nm)/Al:ZnO/MgF_2.

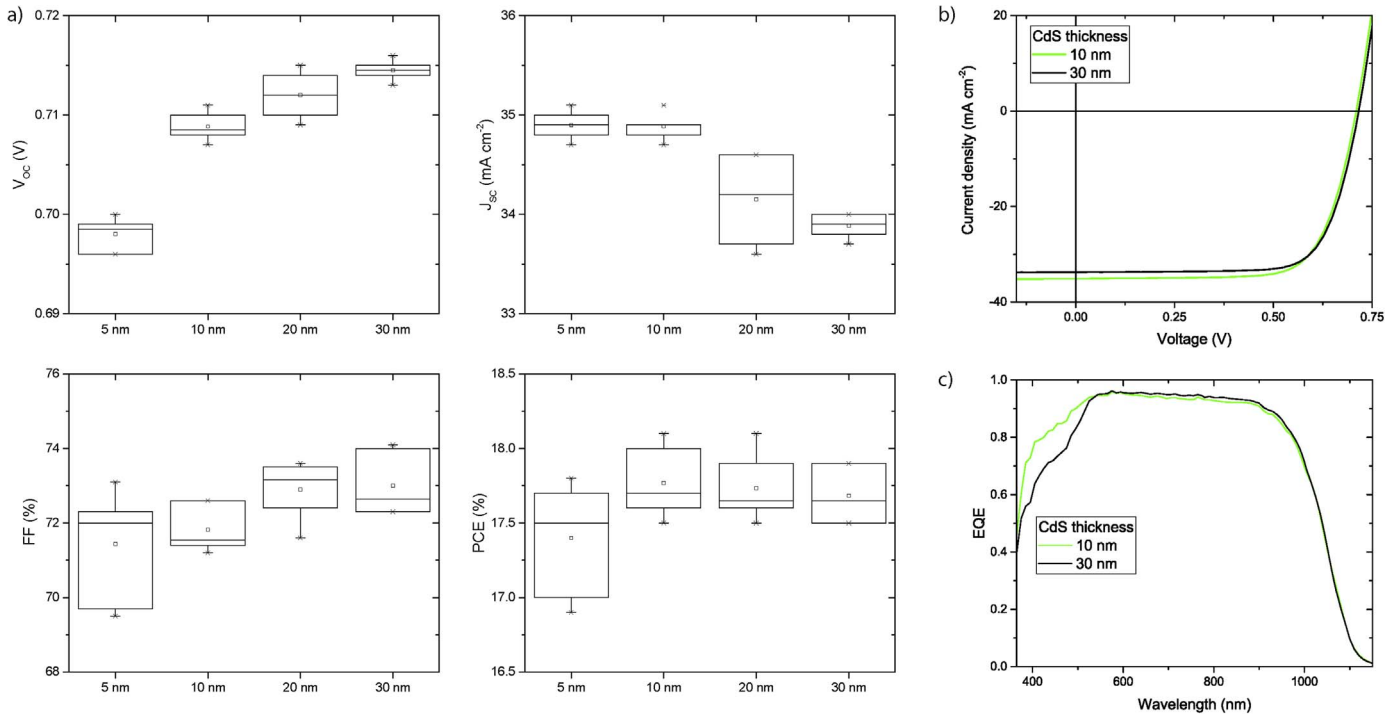

Fig. 4. a) Boxplot chart (6 best performing cells of each sample) of the current-voltage parameters of the device structure SLG/Mo/CIGS/CdS/TiO_2/Al:ZnO/grid(Ni,Al)/MgF_2 with a fixed TiO_2 thickness of 15 nm and a varying CdS buffer layer thickness of 5–30 nm. b-c) corresponding J-V curves and quantum efficiency measurement of representative cells.

To investigate this hypothesis temperature dependent I-V measurements were conducted from 123 K to 323 K (Fig. 7) on CIGS solar cells with either /30 nm CdS/60 nm ZnO/ (reference) or /10 nm CdS/15 nm TiO_2/ buffer layers. At lower temperatures (< 243 K) a strong blocking behavior for the photocurrent, i.e. voltage dependent collection, develops for the latter, which is not seen in a reference sample until about 153 K. This behavior can be related to a reduced thermionic emission of free electrons over a barrier at lower temperatures, e.g. by a positive conduction band offset at the front contact, that becomes detrimental when the electric field strength decreases [26] (1D-simulations will be discussed in this context below). Both structures exhibit another non-ideality, i.e. the change of slope at high voltages (above V_{OC}). This is usually not observed in CIGS solar cells with a NaF PDT but was reported for cells where KF PDT was applied [27]. For both KF and RbF PDT this blocking behavior is not yet understood but may stem from a barrier for the injection current at the front contact, which is correlated to the surface patterning by the PDT on the CIGS surface [28].

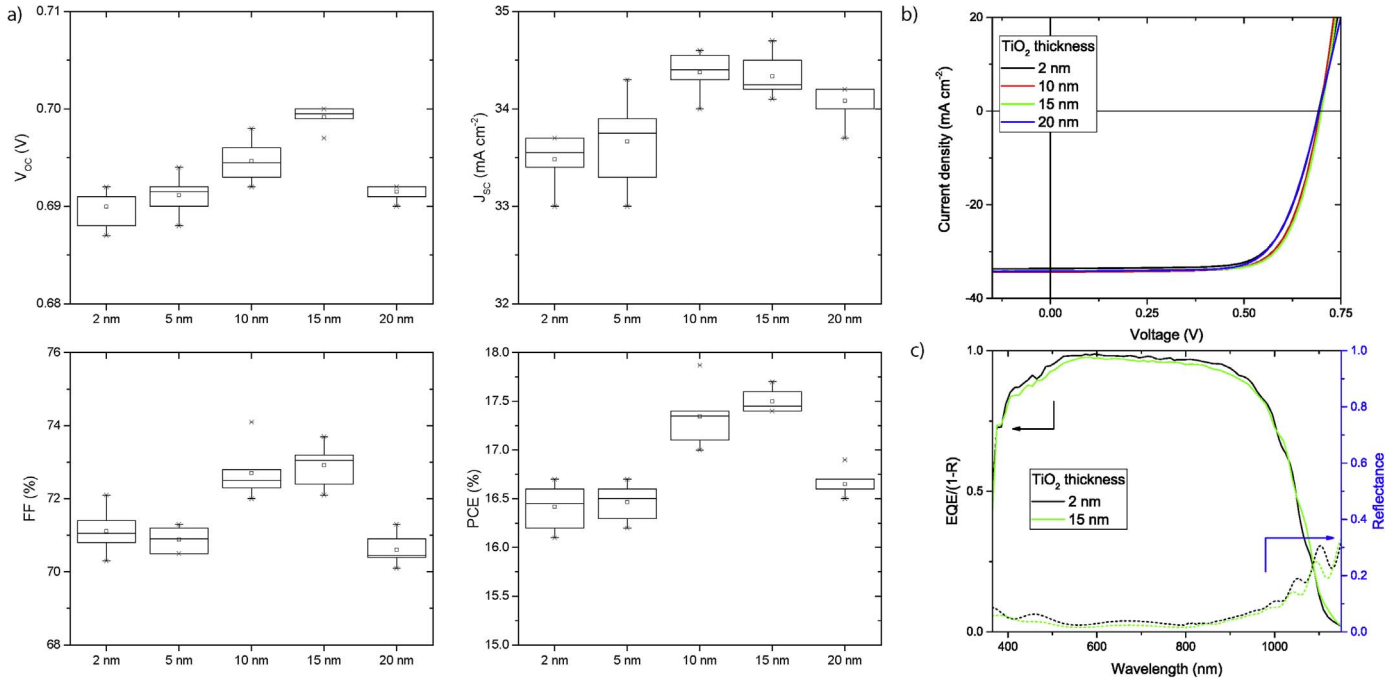

Fig. 5. a) Boxplot chart (6 best performing cells of each sample) of the current-voltage parameters of the device structure SLG/Mo/CIGS/CdS/TiO_2/Al:ZnO/grid(Ni,Al)/MgF_2 with a thin (10 nm) CdS buffer layer thickness and a varying TiO_2 layer thickness of 2, 5, 10, 15 and 20 nm. b-c) corresponding J-V and IQE curves of representative cells.

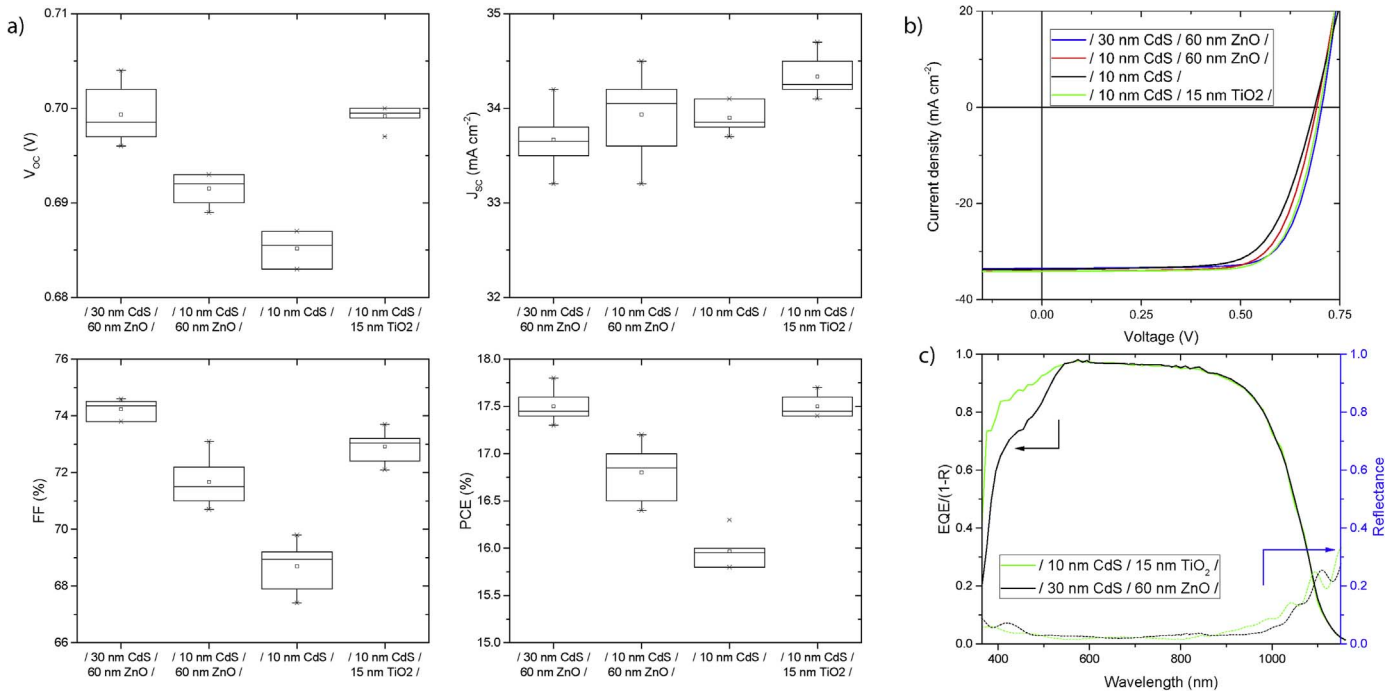

Fig. 6. a) Boxplot chart (6 best performing cells of each sample) for the current-voltage parameters of devices based on the structure SLG/Mo/CIGS/CdS/ZnO or TiO_2/Al:ZnO/grid (Ni,Al)/MgF_2. The reference structure comprising a /30 nm CdS/60 nm ZnO/ buffer layer stack is compared to devices with a thin (10 nm) CdS buffer layer with either a ZnO, a TiO_2 or no HTR layer at all. The absorber layer and all other parameters were the same. b) I-V characteristics of representative cells from plot a. c) IQE and reflectance measurement of cells from graph b.

4. Numerical device modeling

In order to qualitatively understand the observations from the temperature dependent measurements one dimensional numerical simulations were performed using SCAPS [29]. Similar to the work by Inoue et al. [25] the band alignment at the buffer/HTR layer interface is investigated. They concluded that a large positive offset (spike) in the conduction band (ΔE_C(buffer/HTR)~ +0.4 eV) drastically decreases J_{SC} and FF because of the elevated potential barrier to the photocurrent. In order to see the temperature dependency of a barrier introduced by the HTR layer on the I-V characteristics four models (A-D) were simulated from 123 to 323 K at steps of 10 K:

Model **A** is referred to as the reference structure. In model **B** the CdS and ZnO layer thickness was reduced. In **C** a barrier was introduced by reducing the electron affinity of the TiO_2 layer. Model **D** comprises an even higher barrier, carrier concentration and effective density of states. The band diagram is shown in graph E at 298 K and 0 V bias voltage. J-V curves at different temperatures for the four models are displayed in Fig. 8. The parameters for the model layers used for the simulations are given in Table 1. The CIGS model layer has a [Ga]/([Ga]+[In]) grading based on experimental data (see [30]). The defect density of CIGS was adjusted to represent the I-V parameters of the experimental measurements shown in Fig. 7 at 323 K. No external ohmic series or shunt resistance was implemented in the device model.

The focus of the simulations is rather on the band alignment than on the density and position of defect states. A reference model (**A**) is built to represent the device structure comprising a /30 nm CdS/60 nm ZnO/ buffer layer stack. A rather small spike-like conduction band offset between the absorber layer and CdS buffer layer was implemented with +0.16 eV which is in agreement with literature values [31,32]. The

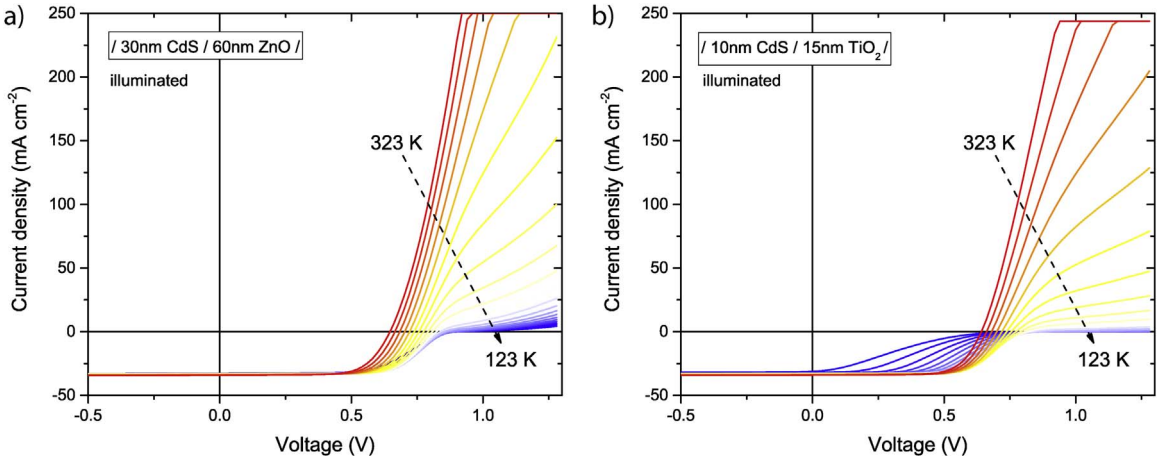

Fig. 7. Temperature dependent I-V measurements of two devices based on the structure SLG/Mo/CIGS/CdS/ZnO or TiO_2/Al:ZnO/grid(Ni,Al)/MgF_2 with the reference structure comprising a /30 nm CdS/60 nm ZnO/ buffer layer stack (a) to which the /10 nm CdS/15 nm TiO_2/ device (b) is compared. It is noted that the device comprising a /10 nm CdS/60 nm ZnO/ buffer layer (not shown here) has comparable temperature dependent I-V characteristics as (a). The measurements were performed from 123 K to 323 K at temperature steps of 10 K.

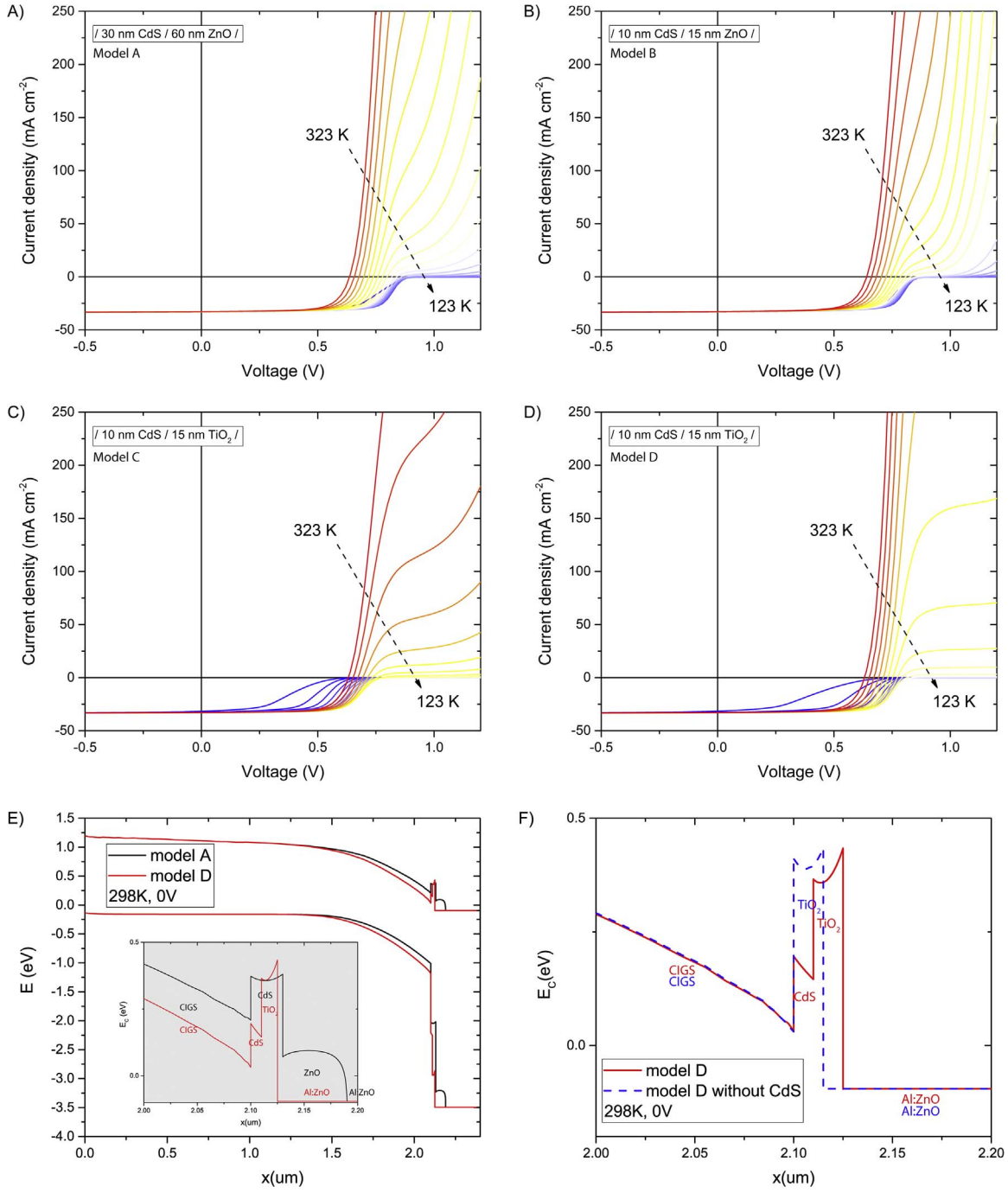

Fig. 8. SCAPS [29] models and simulations of temperature dependent I-V curves. The CIGS layer is graded [30] ([Ga]/([Ga] + [In]) at front surface 0.33, notch 0.23 and back surface 0.5) and a parabolic composition dependence of the band gap and electron affinity (χ) was chosen with a bowing parameter b = 0.2. All defects were neutral (E = 0.6 eV above highest E_V). Temperature dependent I-V measurements of 4 models (**A-D**) were simulated from 123 to 323 K at steps of 10 K. Model **A** is referred to as the reference structure. In model **B** the CdS and ZnO layer thickness was reduced. In **C** a barrier was introduced by reducing the electron affinity of the TiO_2 layer. Model **D** comprises an even higher barrier, carrier concentration and effective density of states. The band diagram is shown in graph E at 298 K and 0 V bias voltage. The conduction band for model **D** is replotted in graph F and compared to a case where the CdS layer is eliminated.

experimentally observed features of this cell are a blocking behavior of the injection current at high voltages when decreasing the temperature from about 293 K, as well as a reduced FF at $T \leq 153$ K (Fig. 8a). In the simulation this feature was implemented by a cliff-like band offset from the CdS to ZnO layer (ΔE_C(CdS/ZnO) = −0.3 eV [31]).

The experimental cell comprising the alternative HTR layer TiO_2 (Fig. 7b) has a reduced layer thickness of both buffer layers. To see if a layer thickness reduction would have a significant influence by itself, in model **B** the thickness of the CdS and ZnO layers are reduced to 10 nm and 15 nm, respectively. The resulting simulated curves show a reduced blocking behavior when compared to the reference model **A**, i.e. the change in curvature at high voltages occurs at lower temperatures. The blocking of the photocurrent at low temperatures observed in the experiment (Fig. 8b) is not yet seen. Hence, in model **C** a further modification was made by introducing a spike-like band offset between the buffer and window layer. In this model TiO_2 is assumed to have a smaller electron affinity (χ) than the ZnO layer which leads to a severe blocking of both the injection and photocurrent when reducing the temperature. However, the injection current is influenced too strongly in model **C** and hence is only partially comparable to the experimental

Table 1
Parameters used for the model layers for the SCAPS [29] simulation. The initial model parameters were motivated from [8,23,25,31–35] and slightly adjusted to represent more closely the experimentally obtained I-V characteristics. Parameter abbreviations: electron affinity (χ), relative dielectric permittivity (ε_r), conduction/valence band effective density of states ($N_{V,C}$), electron/hole mobility ($\mu_{e,h}$), shallow uniform donor/acceptor density ($N_{D,A}$), defect concentration (N_T), capture cross section electrons/holes ($\sigma_{e,h}$).

Parameters	CIGS	CIGS/CdS	CdS	ZnO/TiO_2	Al:ZnO
thickness (nm)	2100		**A**: 30; **B**,**C**,**D**: 10	**A**: 60; **B**,**C**,**D**: 15	250
E_g (eV)	1.05–1.69		2.40	3.30	3.40
χ (eV)	4.77–4.14		4.44	**A**,**B**: 4.75; **C**: 4.23; **D**: 4.22	4.75
ε_r	10		10	10	10
$N_V = N_C$ (cm^{-3})	1E+18		5E+18	**A**,**B**,**C**: 5E+18; **D**: 3E+19	5E+19
μ_e ($cm^2 V^{-1} s^{-1}$)	30		20	50	50
μ_h ($cm^2 V^{-1} s^{-1}$)	15		20	20	20
$N_{D,A}$ (cm^{-3})	2.0E+15		1.0E+17	**A**,**B**,**C**: 1.0E+17; **D**: 6.5E+17	2.0E+21
N_T (cm^{-3})	1.8E+15		1.0E+15		
N_T (cm^{-2})		1.0E+9			
$\sigma_e = \sigma_h$	1.8E−14	1.0E−15	1.0E−14		

data. A better fit was achieved when the barrier height is further increased (reduced χ_{TiO2}) combined with a slightly higher doping concentration and effective density of states ($m^*_{ZnO} \sim 0.3\ m_e$ [33], $m^*_{TiO2} \sim 1\ m_e$ [34]) of the TiO_2 layer as seen in model **D**. In the resulting temperature dependent I-V simulations the strong blocking of the photocurrent could be maintained while influence on the injection current was less severe. On the basis of model **D** the influence of removing the CdS layer was tested, to simulate the effect of pinholes in the CdS buffer layer. All layer properties of model **D** were kept but the CdS layer was removed. At high temperatures no significant difference in the temperature dependent I-V curves was observed. By reducing the temperature the blocking behavior for the photocurrent becomes more severe than in model **D**. This can be explained by a higher effective barrier at the CIGS/TiO_2 interface as seen in Fig. 8F. Although the electron affinity of all layers is unchanged, the presence of CdS, i.e. the potential drop over the CdS layer, shifts the conduction band at the CdS/TiO_2 interface closer to the electron quasi fermi level. To summarize the results of these simulations, a qualitatively good agreement with the experiment is achieved if a spike-like conduction band offset between the CdS buffer layer and the TiO_2 layer is assumed. Fig. 8E is illustrating the conduction and valence band of model **A** and **D**. In the close-up view the offset between CIGS and CdS is the same for both structures. Considering the spike introduced by TiO_2 the blocking of both photo- and injection current can be explained. When comparing model **C** and **D** it becomes clear that no absolute value for the barrier height can be derived since other parameters such as the effective density of states and carrier density of TiO_2 contribute as well to the temperature dependence of the I-V characteristics. The potential drop such a barrier implies would be an explanation for a reduced FF as is experimentally observed.

5. Conclusion

ALD-TiO_2 has proven to be a viable intermediate buffer layer in combination with CdS allowing for a reduction of the CdS layer thickness without adversely effecting efficiency. A gain in current density owing to a reduced parasitic absorption of CdS is observed while the V_{OC} is maintained when compared to a baseline reference cell. Conversely, the application of a 15 nm TiO_2 layer, which is found to be the optimum in terms of I-V performance, leads to a reduced fill factor. In temperature dependent I-V measurements a strong photocurrent blocking behavior was observed in a cell comprising a /10 nm CdS/15 nm TiO_2/ buffer layer stack at lower temperatures (< 253 K). Numerical simulations suggest a possible origin of this behavior is a positive conduction band offset at the CdS/TiO_2 interface. Assuming a fixed barrier height, an improvement of the FF and hence device performance would be realized by an increased carrier concentration and effective density of states which could be achieved by doping of the TiO_2 layer.

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Appendix A. Supporting information

Supplementary data associated with this article can be found in the online version at http://dx.doi.org/10.1016/j.solmat.2017.09.030.

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