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Title

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Abstract

Potassium post deposition treatment (K-PDT) has been a major breakthrough for CIGSSe ($Cu(In,Ga)(S,Se)_2$) solar cells yielding world record efficiencies. K-PDT yields significant improvements in open circuit voltage, fill factor and CdS coverage leading to efficiencies above 20% for CIGSSe material. Here we present a similar K-PDT approach for solution processed kesterite solar cells. K-PDT improves the open circuit voltage of kesterite solar cells, however a severe blocking of the short circuit current and reduction of fill factor reduces the overall device efficiencies. Furthermore, quantum efficiency measurements indicate that K-PDT alters the properties of the CdS layer whereas time-resolved photoluminescence measurements exhibit an additional third exponential component, which can be attributed to minority carrier trapping at the interface.

Keywords: thin film solar cells, kesterite, solution processing, Voc-deficit, post deposition treatment.

1. Introduction

Kesterite ($Cu_2ZnSn(S,Se)_4$) is a promising absorber material due to its earth abundant and non-toxic constituents. Despite continuous improvements in device efficiencies, peaking at 12.6 % [1], a comparably high open circuit voltage deficit (V_{OC}-deficit) remains the major culprit hindering further advancements [2,3]. The major source of the V_{OC}-deficit is still under debate, especially whether the main recombination paths are located in the bulk, grain boundaries or interfaces of the device. Alkali metal incorporation into the absorber layer has shown significant improvements of bulk properties by enhancing grain growth, increasing doping concentration and passivating grain boundaries in the case of sodium [4–6]. Other bulk alkali dopants have also been reported but their impact on electronic properties and device performance is more ambiguous [7–9]. So far, alkali post deposition treatment of the kesterite absorber has not been thoroughly investigated yet. In the closely related absorber material CIGSSe ($Cu(In,Ga)(S,Se_2)$) potassium treatment of the absorber surface yielded significant improvements in V_{OC} and fill factor (FF) leading to new record efficiencies above 20% for this material [10–11].

Here we study the effect of potassium post deposition treatment (K-PDT) on kesterite absorber layers. The absorber layers are prepared by a dimethyl sulfoxide (DMSO) solution process described elsewhere [12]. Various thicknesses of potassium fluoride (KF) were evaporated onto the absorber layer, followed by an annealing at 350 °C in selenium atmosphere, which are similar processing parameters as for the K-PDT in CIGSSe absorber layers. A significant difference in the methodology, however, is that in this study the KF evaporation is conducted at room temperature in a separate evaporation chamber following a transfer in ambient atmosphere whereas in the original CIGSSe K-PDT process the KF evaporation takes place at elevated temperatures without breaking the vacuum directly proceeding the absorber layer growth process.

Systematic electrical characterization of absorbers and finished solar cells with scanning electron microscopy (SEM), current-voltage measurements (J-V), external quantum efficiency (EQE) and time-resolved photoluminescence (TRPL) are used to identify the effect of KF-PDT on kesterite solar cells.

2. Experimental details

The precursor solution consisted of thiourea (99 %+, Sigma-Aldrich), $SnCl_2 \cdot 2H_2O$ (98 %, Sigma-Aldrich), $ZnCl_2$ (99.99 %, Alfa Aesar), $CuCl_2$ (98 %+, Alfa Aesar) and NaCl (99.99 %, Alfa Aesar), dissolved in DMSO (99.9 %, Alfa Aesar). The precursor solution contained 0.1 M NaCl and the molar ratios were Cu/(Zn+Sn) = 0.66 and Zn/Sn = 1.08. The precursor solution was spin-coated onto a Mo coated soda-lime glass and dried on a hotplate with 320 °C in air. The spin-coating and drying steps were repeated several times in order to obtain the desired precursor film thickness of 1.5 – 2 µm. All samples were annealed in an Annealsys AS ONE 150 RTP furnace inside a closed graphite box with selenium pellets (800 mg). The temperature gradient employed for annealing was the 3-stage process with holding temperatures at 300 °C, 500 °C and 550 °C. Metal ratios of the selenized absorbers were: Cu/(Zn+Sn) = 0.83 and Zn/Sn = 1.24. All metal ratios were obtained by X-ray fluorescence measurements calibrated by inductively coupled plasma mass spectrometry.

After selenization the absorbers were immersed for 30 s in a 10 wt% KCN solution in order to remove copper-rich phases and clean the surface from contaminations and oxides. Following the KCN etching, a KF layer with thicknesses varying between 0.25 nm to 60 nm were evaporated on top of the absorber layer. Immediately after the evaporation the absorbers were transferred back into the graphite box used prior for selenization and annealed at 350 °C (1 °C/s ramping, 500 hPa N_2 background pressure) in selenium atmosphere (200 mg Se pellets added into the graphite box) for 20 minutes, followed by natural cooldown to room temperature. A 50 nm - 60 nm thick CdS buffer layer was deposited by chemical bath deposition, and 70 nm/350 nm i-ZnO/Al:ZnO bilayer was sputtered. A Ni/Al top grid was deposited by e-beam evaporation. The sample with 0 nm KF was not exposed to any kind of treatment in between KCN etching and window layer deposition. Individual solar cells were mechanically scribed to an area of 0.30 ± 0.02 cm^2. Finally, post-annealing of complete devices at 120 °C for 60 minutes in air was performed.

SEM measurements were done on a Hitachi S-4800 electron microscope. The J-V characterization was performed under standard test conditions (100 $mWcm^{-2}$, 25 °C, AM1.5G) using a solar simulator calibrated with a certified Si diode. The EQE spectra were recorded using a chopped white light source (900 W halogen lamp) with a LOT MSH-300 monochromator, which was calibrated with certified Si and Ge diodes. The illuminated area on the sample was 0.1 cm^2 including grid lines. Room temperature TRPL was measured on a FT300 fluorescence lifetime spectrometer from PicoQuant with a 639 nm pulsed diode laser as excitation source (pulse width 90 ps, repetition rate 10 MHz) and a thermoelectric cooled Hamamatsu near infrared photomultiplier tube module H10330A-45 (rise time 0.9 ns, transit time spread 0.4 ns).

3. Results and discussion

Fig. 1 presents the photovoltaic parameters of all samples with statistics being derived from 9 cells for each KF thickness. In Fig. 1 A) the J_{SC} remains around 34 $mAcm^{-2}$ for the samples with up to 1 nm KF thickness and decreases when further increasing the amount of KF. Additionally, the J_{SC} values for the same KF thickness start to spread considerably. A qualitatively similar behavior is observed for the FF and the efficiency, which are up to 9.7 % for the baseline with 0 nm KF (no anti reflective coating was applied to all samples). The V_{OC} shows an upwards trend with 5 nm KF thickness and more. For the samples with 25 nm and 60 nm KF the spread in the values for each thickness becomes increasingly bigger so only the best cells show the improved V_{OC}.

The described trends are also evident in the J-V – curves presented in Fig. 2. The shape of the curves with thicker KF layer indicates that the source of this current blocking behavior originates from a barrier. This barrier could be caused by an insulating layer formed during the K-PDT or KF alters the electrical properties of CdS. This is different to the CIGS case that neither exhibits a current blocking behavior nor a distinct impact on the electrical properties of the CdS layer and the K-PDT results in a copper-poor interface layer constituted of K, In and Se that reduces interface recombination and improves CdS growth properties [13].

The EQE of all samples is shown in Fig. 3. The reduction of the J_{SC} in Fig. 1 A) stems from an overall reduction of carrier collection throughout the whole wavelength range. In the short-wavelength region from 375 nm to 550 nm, which is partly absorbed by the CdS layer with a bandgap of 2.4 eV, an abnormal behavior of the EQE signal exceeding unity can be observed for the samples with ≥ 10 nm KF thickness. From our observation this artifact could be attributed to the increased photoconductivity of CdS as a result of the incorporation of alkali impurities [14]. During EQE measurements the incident light that is modulated by a certain frequency and absorbed in the CdS layer changes the conductivity of that layer with the same frequency. The modulated conductivity of the CdS layer modulates part of the photocurrent originating from the bias light and is eventually falsely interpreted by the lock-in amplifier as photocurrent arisen from the chopped light source [15]. The increased EQE signal in this short wavelength region is therefore a measurement artifact and does not represent the collection probability of electron-hole pairs and is conclusively not observed in J-V measurements. Without the bias light, the abnormal behavior disappears.

To verify that the current blocking behavior is not caused by a very thick CdS layer or other changes in growth SEM cross sections of all devices were examined and all CdS layers have shown similar thickness of 50 nm – 60 nm. Also no obvious change in the morphology of both the absorber layer and the thin CdS were detectable as can be depicted from Fig. 4.

Finally TR-PL measurements for all samples were conducted and fitted with a two exponential equation, whereas the first exponent describes the separation of holes and electrons due to the built-in potential and the second exponent the minority carrier lifetime [16]. The derived minority carrier lifetimes are in the range from 5 to 7 ns without any obvious trend in regards to the KF layer thickness. However, the samples with 10 nm KF and more exhibit a slower decay after 30 ns compared to the samples with less KF as shown in Fig. 5 for representative cells with 0 nm and 60 nm KF thickness. The sample with 0 nm KF can be adequately fitted by a two exponential decay but the sample with 60 nm shows a significant deviation. A reasonable fit could only be

obtained when including a 3rd exponential with an average lifetime of 20 ns, that we assume is caused by trapping and reemission of carriers [17]. The trapping of carriers also lowers the derived minority carrier lifetime so that the aforementioned results for τ_2 can be expected to be higher for samples with more than 10 nm KF thickness and would therefore be in agreement with the improved V_{OC} for these samples.

4. Conclusion

Potassium post deposition treatment of solution processed solar cells with various KF thicknesses exhibits a decrease in short circuit current, fill factor and efficiency with increasing KF thickness that originates from a severe blocking of the photocurrent. However, the open circuit voltage is improved suggesting a decrease of interface recombination. The CdS buffer layer growth was not affected but the buffer layer shows a significant photoconductivity effect in external quantum efficiency measurements. Furthermore, minority carrier trapping appears for thicker KF thicknesses indicating the formation of trap states at the absorber/buffer interface.

We conclude that KF-PDT improves the V_{OC} but the different surface chemistry compared to the CIGSSe case does not yield the same beneficial interface layer. In order to get a better insight to the chemical nature of the modified interface further experiments utilizing for example XPS measurements should be conducted. Modifications of the process parameters or a change in surface chemistry are needed to obtain an overall benign effect on device performance.

Acknowledgements

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Figures captions

Fig. 1: Photovoltaic characteristics of K-PDT treated samples with KF thickness varying from 0 nm to 60 nm.
A) J_{SC} decreases similar to FF (B) and efficiency η (C) with KF thickness 5 nm and more. V_{OC} increases with KF thickness of 5 nm and more, however for 25 nm and 60 nm the V_{OC} data is spreading significantly and only the best cells show an improved V_{OC}.

Fig. 2: J-V – curves of the best cells treated with K-PDT and varying KF thickness from 0 nm to 60 nm. The J-V – curves show the blocking of J_{SC}, reduction in FF and increase in V_{OC} with increasing KF thickness. The shape of the curves indicates that the source of this current blocking behavior originates from a barrier.

Fig. 3: External quantum efficiency of the best cells treated with K-PDT and varying KF thickness from 0 nm to 60 nm. The reduction in J_{SC} originates from a decreased collection for all wavelength. For KF ≥ 10 nm the EQE shows an abnormal signal peak in the wavelength region from 375 nm to 550 nm that is an

artifact which is probably related to the increased photoconductivity of the CdS layer due to K incorporation.

Fig. 4: SEM cross section images of the finished devices with 0 nm KF (A) and 60 nm KF (B). The morphology of both absorber layers is similar and was therefore not altered by the K-PDT process. The thin CdS layer thickness was determined to 50-70 nm for both samples indicating no change in CdS growth velocity due to KF presence at the surface.

Fig. 5: Time-resolved photoluminescence measurements on the samples with 0 nm (A) and 60 nm (B) KF thickness. Whereas the 0 nm sample can be fitted well with two time constants τ_1 and τ_2 the fit for the sample with 60 nm KF shows a significant deviation. This deviation can be attributed to charge carrier trapping and reemission and only occurs for samples with ≥ 10 nm KF.

Figures

Fig. 1.

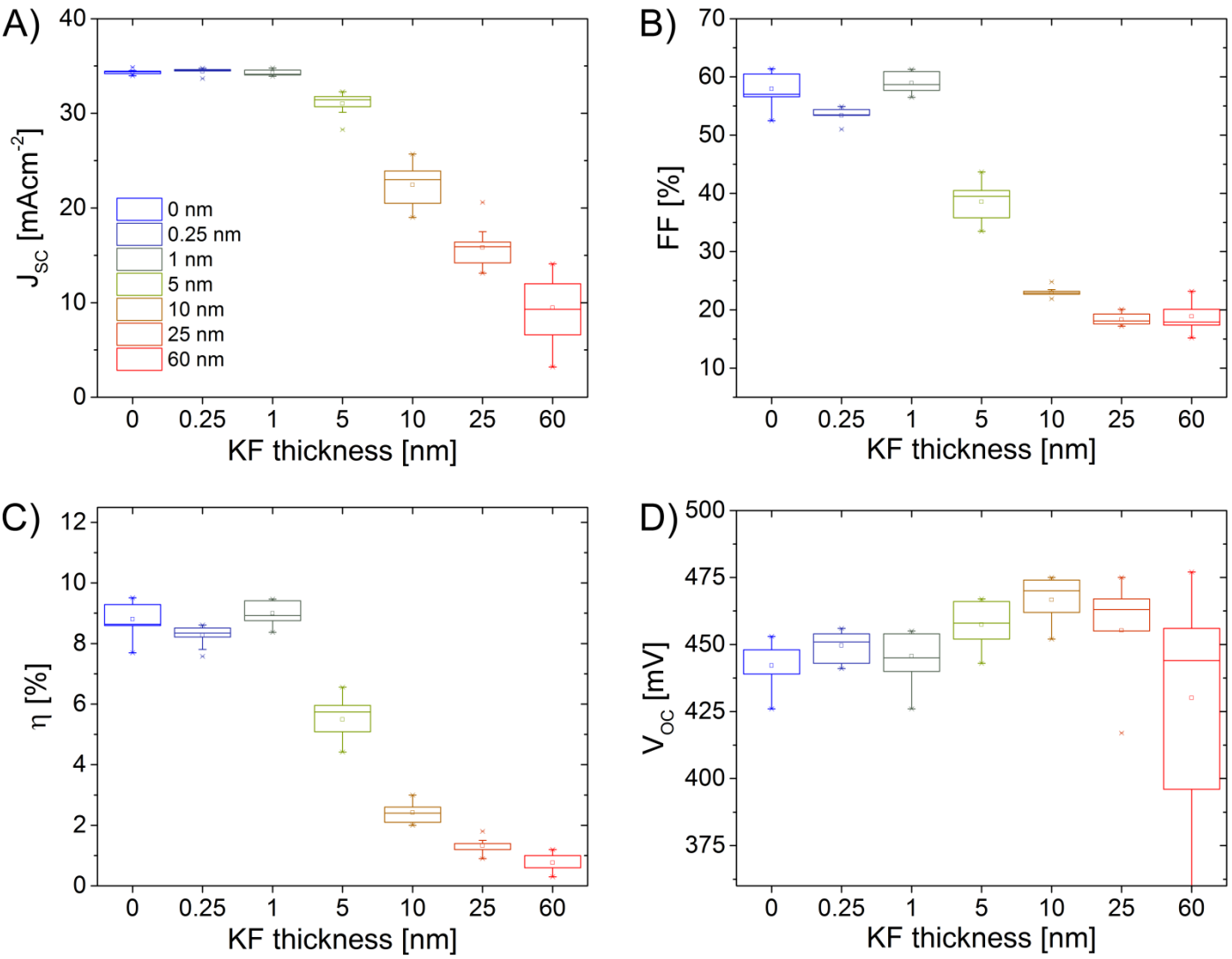
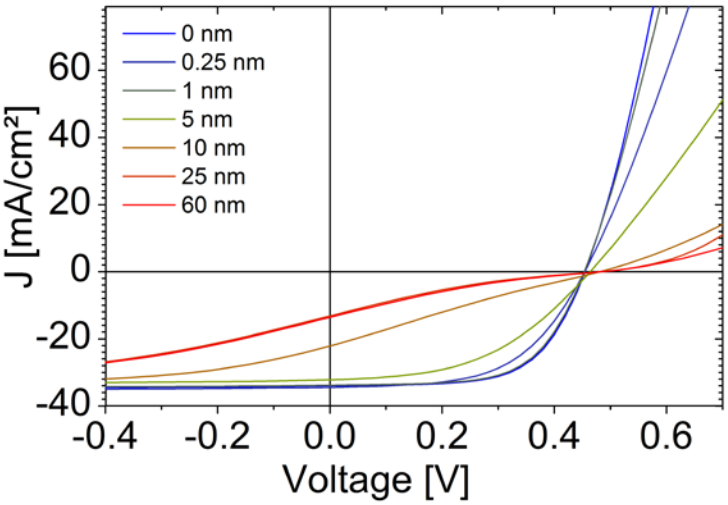


Fig. 2.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1 nm
5 nm
10 nm
25 nm
60 nm
J [mA/cm²]
60
40
20
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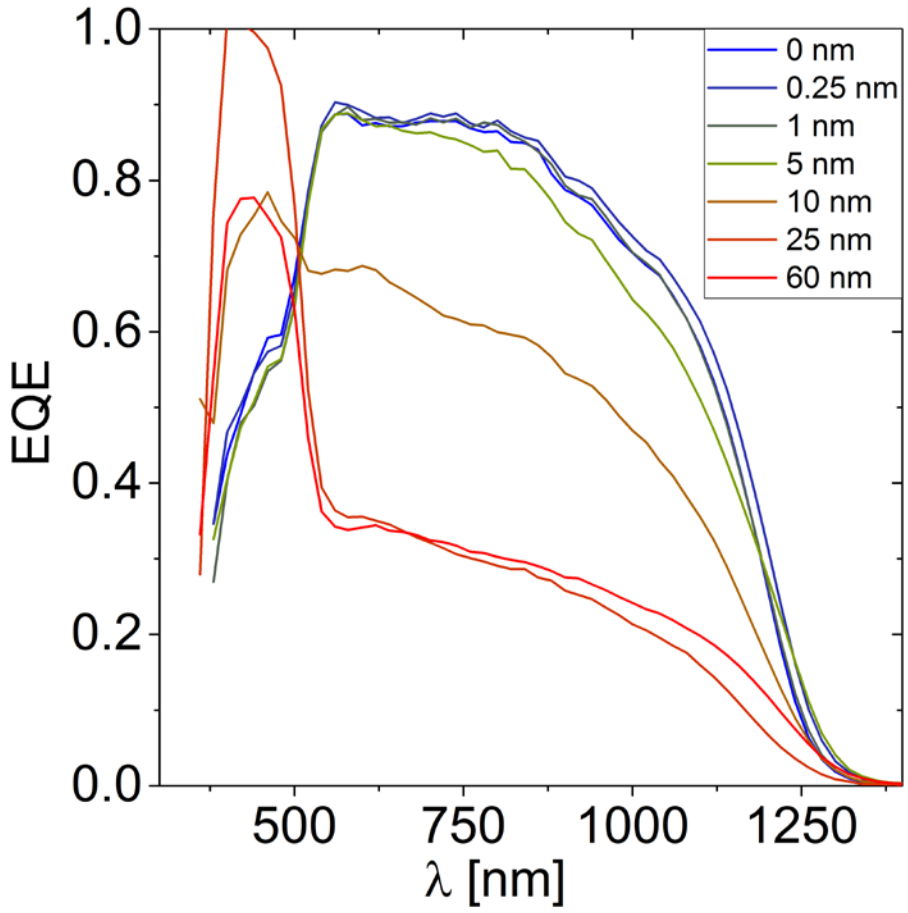
-20
-40
-0.4
-0.2
0.0
0.2
0.4
0.6
Voltage [V]

Fig. 3.


0 nm
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1 nm
5 nm
10 nm
25 nm
60 nm
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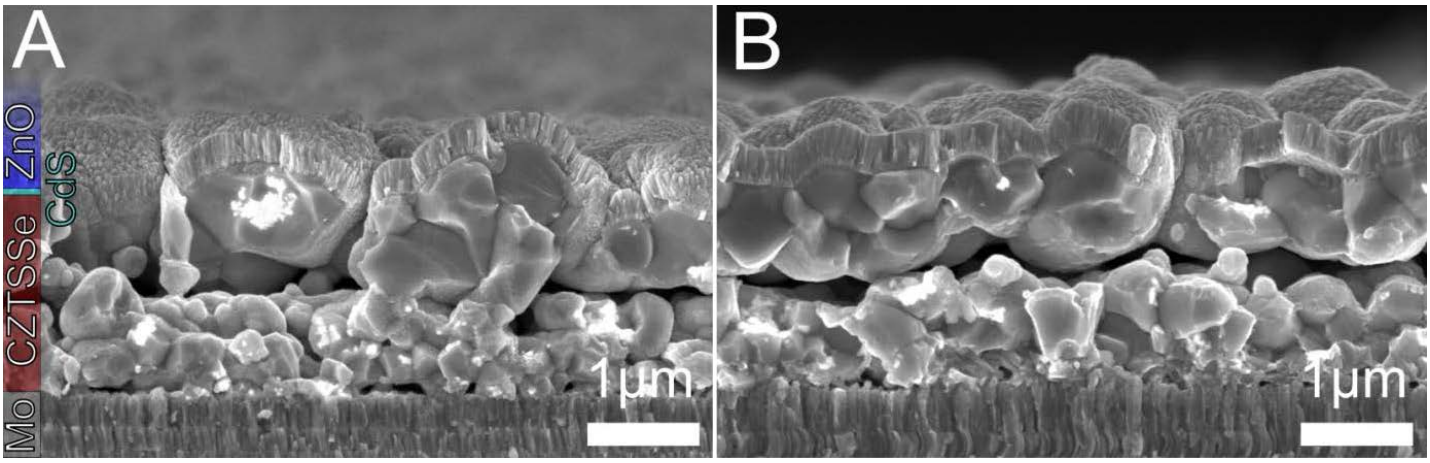
1000
1250
λ [nm]

Fig. 4.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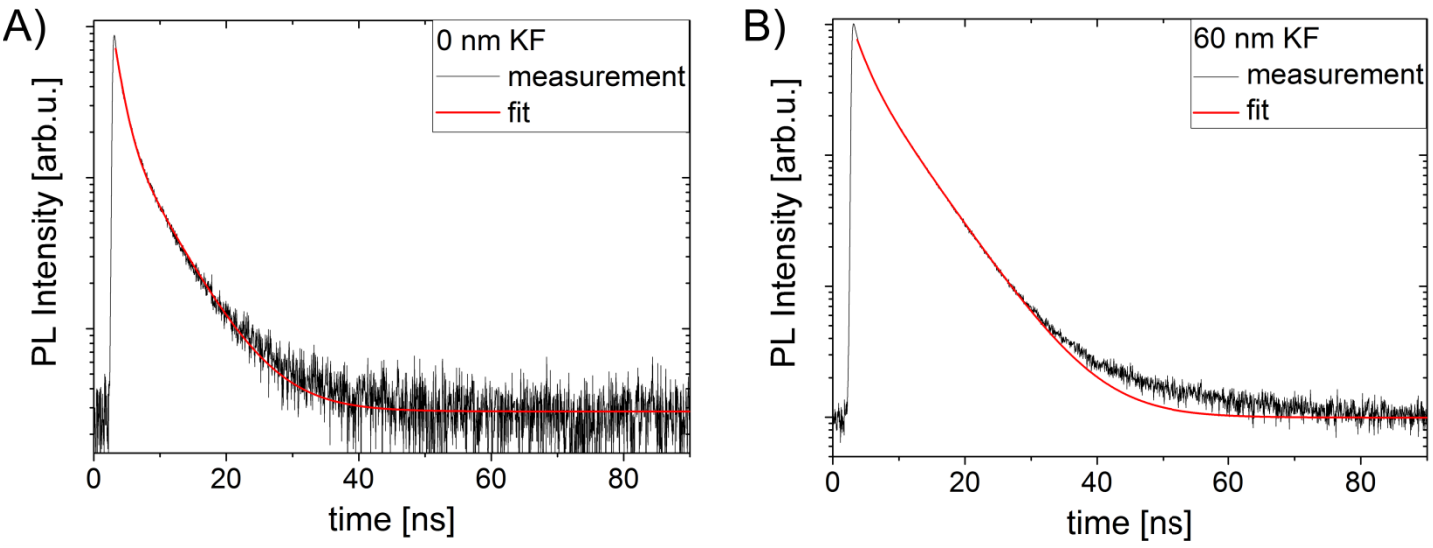
CdS
CZTSSe
Mo
1µm
B
1µm

Fig. 5.


A)
0 nm KF
measurement
fit
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40
60
80
time [ns]
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60 nm KF
measurement
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