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Injection Current Barrier Formation for RbF Postdeposition-Treated Cu(In,Ga)Se_2-Based Solar Cells

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Among the thin-film solar cell technologies, Cu(In,Ga)Se_2-based solar cells demonstrate the highest efficiencies, where the recent boost in efficiency is triggered by a KF postdeposition treatment (PDT). In this contribution, Cu(In,Ga)Se_2-based solar cells are fabricated using RbF PDTs after absorber layer growth with varying substrate and RbF source temperature. The electronic charge transport properties of the solar cell devices are investigated using temperature-dependent current–voltage analysis and admittance spectroscopy. To investigate the observed transport barriers, a novel concept based on the differential series resistance is proposed. This approach is supported by simulations of current–voltage curves, which reproduce qualitatively experimental data. Experimentally, two parallel conduction paths are found, which act as barriers with different activation energies and impede the charge carrier transport. Both the thickness and height of these barriers increase with an increasing amount of incorporated Rb and can lead to losses in the fill factor and power conversion efficiency at room temperature. Etching in HCl prior to CdS buffer layer deposition reduces the barrier width and can recover these losses.

1. Introduction

Cu(In,Ga)Se_2 (CIGS) solar cells recently achieved a world record efficiency of 22.8%, which is the highest among the thin-film solar cell technologies.[1] A strong boost in efficiency was enabled due to the addition of a KF postdeposition treatment (PDT).[2] Recently, the addition of Rb and Cs has proven to be beneficial for device performance as well, and a 22.6% efficient CIGS device has been demonstrated using a RbF PDT.[3] The impact of the KF PDT has been investigated by several groups and mainly a modification of the CIGS surface was observed. Initially, it was found that the KF PDT causes the Cu depletion of the CIGS surface[4] and that a K-In-Se phase forms.[5–8] Additionally, a widening of the surface bandgap was found after the KF PDT[8,9] which is beneficial in case of interface recombination at (or close to) the heterointerface with the buffer layer.[10] However, also a beneficial effect on the bulk properties was identified. Nicoara et al. found an upward bending of the conduction band at grain boundaries.[11] Jensen et al. showed by photoluminescence reduced potential fluctuations after KF PDT;[12] however, effects due to interference were not taken into account.[13,14] Also an impact on the doping density[7,15–17] and the formation of a barrier for the diode current[15] have been observed.

As mentioned above, heavier alkalines have a beneficial effect on the device efficiency as well when added as a PDT.[3] In this contribution, we investigate the influence of a RbF PDT by electrical characterization techniques such as temperature-dependent current–voltage measurements and admittance spectroscopy. Especially, we explain the origin of the commonly observed capacitance step for CIGS-based absorbers and the blocking of the diode current. Concerning the origin of the capacitance step, which is generally labeled "N1," a controversial discussion in literature exists. It was assigned to a bulk deep defect,[18] a minority carrier trap state close to the absorber/buffer heterointerface[19] or to a barrier for the diode current.[20] An additional correlation to the blocking of the diode current was reported by several groups, which strengthens the origin to be due to a barrier.[15,20–22]

2. Quantification of an Injection Barrier

A barrier for the injection current generally introduces a nonideal diode behavior, i.e., the current–voltage curve cannot be described by the one-diode model. In the case of a back barrier, for instance, a roll-over and current saturation of the I–V curve is expected.[23] For a barrier positioned at the front contact, the situation is more complicated as the barrier might also be dependent on illumination, and voltage[24] and a current saturation is not necessarily observed.

In Section 3.3, the differential series resistance in forward bias is used to quantify the barrier responsible for the blocking of the diode current. In order to verify that approach simulations are carried out using Sentaurus TCAD (see Section 6 for more details). The band diagram of the simulated structure is

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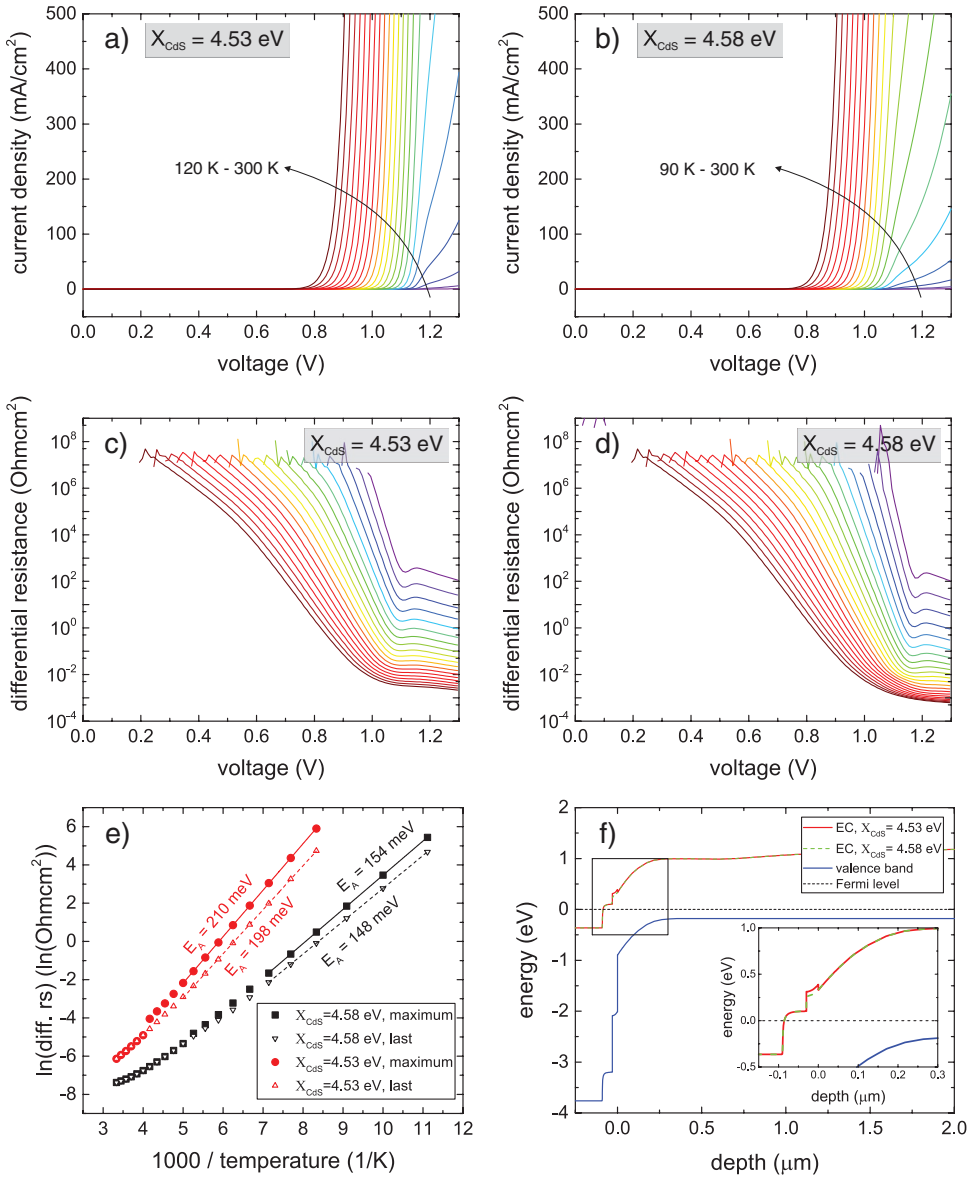

Figure 1. Simulation results of IVT curves. A barrier has been introduced to be at the iZnO/CdS caused by a conduction band offset, see (f). The magnitude of the barrier was adjusted by the electron affinity of CdS X_{CdS}. a) and c) show the *I–V* and differential series resistance curves for X_{CdS} = 4.53 resulting in a conduction band offset of 210 meV. b) and d) are the *I–V* and differential series resistance curves for X_{CdS} = 4.58 having a conduction band offset of 160 meV. Extracted values for each temperature are plotted in an Arrhenius diagram in e). Solid symbols represent values determined from the local maximum of the differential series resistance in forward bias and at lowered temperatures. Open symbols are extracted by the value at 1.3 V (last points). The activation energy was determined from the slope of fitted straight lines.

shown in **Figure 1**f. A barrier at the front contact is introduced originating from a conduction band offset ΔE_C at the iZnO/CdS interface.

It needs to be stressed that for the simulation, it is not important which interface shows the conduction band offset. In principle, the barrier (in the form of a conduction band offset) could also be located at the CdS/CIGS interface, for instance, due to a CIGS-surface layer. In fact, such a surface layer is assumed based on experimental results to cause the barrier (see Section 4).

In the simulations, a variation of the barrier height is achieved by a variation of the electron affinity X_{CdS} of CdS. Simulated temperature-dependent *I–V* (IVT) curves are shown in Figure 1a,b for X_{CdS} equals 4.53 meV (ΔE_C = 210 meV) and 4.58 meV (ΔE_C = 160 meV), respectively. For 4.58 meV (ΔE_C = 160 meV), the temperature range is extended to lower temperatures in order to see the impact of the barrier more clearly. From the *I–V* curves, the differential series resistance is calculated according to

$$r_{s,diff} = \frac{dV}{dJ} \quad (1)$$

and plotted in Figure 1c,d. For small forward bias voltages, the reverse saturation current density dominates, causing large

values of the differential series resistance. Due to numerical inaccuracies, scattering of the simulated current values introduces a large scattering for the differential series resistance. The differential series resistance is therefore cut for a certain voltage (and not plotted over the entire voltage range starting from 0 V). The strong decrease of $r_{s,diff}$ over several orders of magnitude is caused by the onset of the diode current. The leveling-off at high forward bias (above 1 V) and at high temperatures (300 K) is due to the series resistance introduced by the hole conductivity of the absorber. For lowered temperatures, the differential series resistance shows a local maximum around 1.1–1.2 V, which is caused by the barrier, i.e., the conduction band offset ΔE_C. To quantify the barrier height, certain values of $r_{s,diff}$ are extracted and plotted in an Arrhenius diagram as displayed in Figure 1e. Solid symbols represent values extracted from the local maximum (if present) around 1.1–1.2 V. For higher temperatures, the local maximum is not observed, and the last point at 1.3 V is used. Open symbols are always taken from the value at 1.3 V. The activation energy of $r_{s,diff}$ (the barrier height) is extracted from the slope of a fitted straight line through the linear part at low temperatures. The activation energies obtained from the local maximum (solid symbols) show very good agreement with the conduction band offsets (see Figure 1f). In contrast, the fits of the values taken at 1.3 V slightly underestimate the activation energy. At high temperatures, a deviation of the straight line is observed in the Arrhenius diagram (Figure 1e), which is caused by the current to be limited by the CIGS bulk conductivity as mentioned above and not by the barrier.

We note that the simulated curves of $r_{s,diff}$ are in good qualitative agreement with the experimental curves shown in Figure 4e. Consequently, the barrier for the experimental curves is estimated by using the local maximum of the differential series resistance in forward bias. Additionally, the shape of the curves hints to the fact that the barrier for the experimental curves is located at the front contact, as a saturation of the current is expected for a barrier located at the back contact as mentioned above.[23]

3. Results

3.1. Device Performance

Figure 2 shows a boxplot of the *I–V* parameters for devices stemming from the source temperature series. The statistics of the parameters result from 18 individual solar cell devices on one substrate. An increasing open-circuit voltage (V_{OC}) is achieved for increasing RbF source temperatures up to 500 °C. Within the same temperature range, the short-circuit current density (J_{SC}) does not vary systematically. The fluctuations might be due to the fact that no anti reflection coating (ARC) is applied and due to small process inhomogeneities. The fill factor (FF) however decreases for temperatures above 490 °C due to a formation of a barrier for the injection current (see Section 3.3). As a consequence, only a small increase in efficiency is observed for source temperatures between 480 and 500 °C

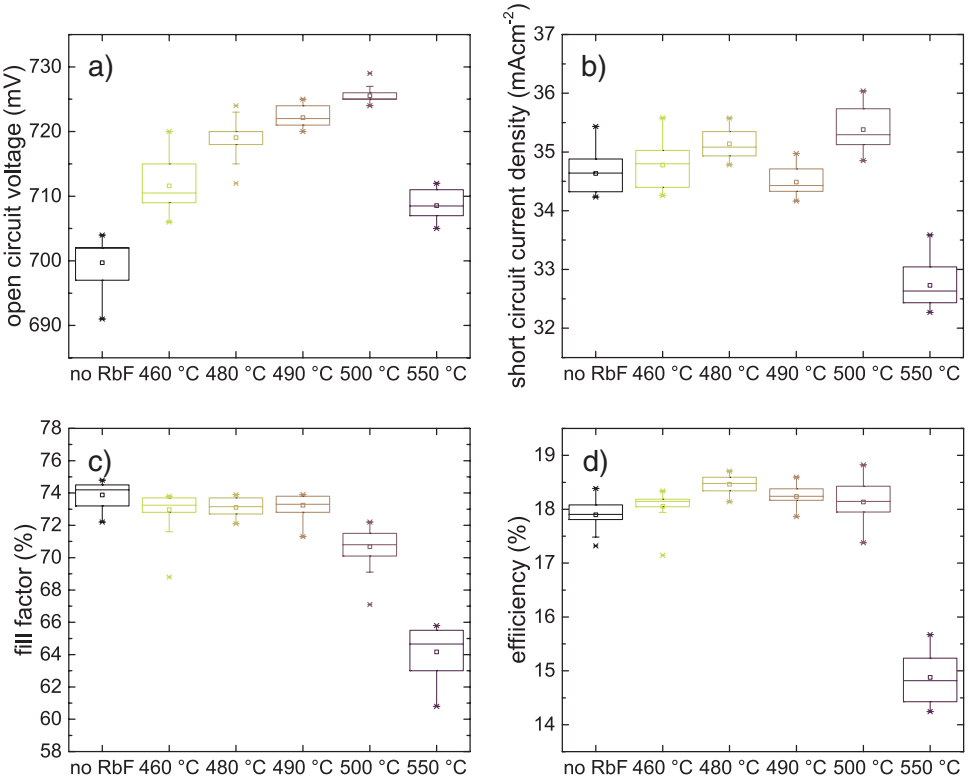

Figure 2. *I–V* parameters for the devices from the RbF source temperature series. The substrate temperature was set to 250 °C during PDT. Up to a RbF source temperature of 500 °C, an increase in the V_{OC} is observed. However, as the FF is decreasing, no strong increase in efficiency is observed. All devices are analyzed without an ARC.

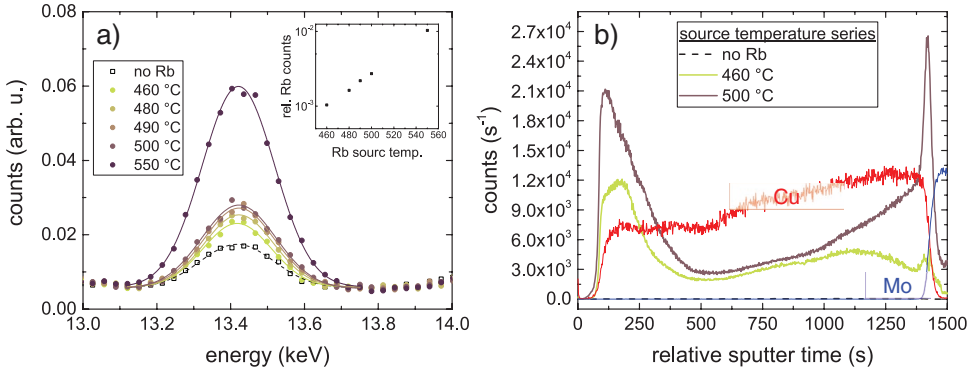

Figure 3. a) Measured XRF signal of the $K\alpha 1$ signal of Rb (solid circles) of the source temperature series. Solid lines represent Gaussian fits of the data. Open squares and dashed line represent a measurement and a fit of a solar cell without a RbF PDT. The area under the fit line is taken as the amount of incorporated Rb into the solar cell, which shows an exponential increase with respect to the RbF source temperature as shown in the inset. b) Shows the SIMS measurements of three devices indicating that the excess Rb accumulates mainly at the front and back contact of the absorber. Only a small increase of Rb is observed in the bulk of the absorber. Cu and Mo profiles were added for the 500 °C sample to indicate the absorber front and back side.

compared with the lowest temperature of 460 °C (or no RbF). The decrease of all solar cell parameters for a source temperature of 550 °C might be due to the formation of a strong barrier as will be shown in Section 3.3.

A similar trend of the *I*–*V* parameters is observed for the substrate temperature series. An increase in V_{OC} is observed, which is however accompanied by a decreasing FF (see Figure S1, Supporting Information).

The parameters for the RbF washing series are shown in Figure S2 in the Supporting Information. The RbF source temperature was rather high (520 °C) and consequently, the standard device consisting of a H_2O wash shows a low FF of roughly 70%. After a HCl etch, the FF can be recovered leading to an increased efficiency. The reason for the increased FF after HCl etch will be discussed in Section 3.3 and Section 4.

The highest efficiency for the devices of all series is achieved with a substrate temperature of 230 °C, a RbF source temperature of 500 °C, and a H_2O wash prior to CdS deposition. The following *I*–*V* parameters were measured: V_{OC} = 721 mV, J_{SC} = 35.3 mA cm^{-2}, FF = 74.8%, resulting in an efficiency of 19.05% (w/o ARC).

3.2. Rb Distribution

X-ray fluorescence (XRF) is measured on completed devices to quantify the amount of incorporated Rb into the solar cell. For that purpose, the $K\alpha 1$ peak of Rb at 13.395 keV is quantified, which is shown in **Figure 3**a. The spectra are normalized to the Se peak prior to the analysis. Subsequently, the Rb peak is fitted with a Gaussian curve to determine the area under the peak. A sample, which did not underwent a RbF PDT (labeled "no Rb"), is measured as well and also shows a Rb signal. This signal was determined to come from the glass substrate from a dedicated experiment. Therefore, the same contribution is expected for the other samples. To obtain the Rb signal from the absorber only, the fitted signal from "no Rb" is subtracted from the other fitted signals. This quantity is plotted in the inset of Figure 3a and follows an exponential behavior indicating an exponentially increased amount of Rb in the absorber layer with increasing RbF source temperature. To investigate the location of the excess Rb, secondary ion mass spectrometry (SIMS) profiles are recorded for the devices without a RbF PDT (sample: no Rb) and with a source temperature of 460 and 500 °C. The Rb profiles are shown in Figure 3b including the Cu and the Mo signal to indicate the front and backside of the absorber. Clearly, the additional Rb strongly peaks at the front and back, while only a small increase is observed within the bulk of the absorber. The RbF PDT leads to a Rb-rich front surface[25] similar as for a KF PDT,[26] which could explain the Rb peaks in the SIMS profile toward the front surface. In particular, a Rb-In-Se layer is observed on top of the CIGS absorber, even though a higher amount of Cu might be present in this layer[25] compared to the K-In-Se layer.[4] A clear Cu depletion at the front surface could not be observed based on SIMS profiling but was found by X-ray photoelectron (XPS).[25] Possibly due to the presence of Cu in the surface layer,[25] the SIMS profiles do not show a clear Cu depletion.

The Rb profile of the sample, which did not underwent a RbF PDT (dashed line in Figure 3b), is flat—as expected—and confirms that the XRF signal for that sample shown in Figure 3a does not arise due to contamination of Rb in the absorber, but due to the glass substrate.

3.3. Injection Barrier Formation

The evolution of the IVT curves under illumination for three samples of the RbF source temperature series is shown in **Figure 4**a–c. Clearly, an increasing blocking behavior of the injection current is observed when increasing the amount of Rb incorporated into the solar cell device (note that a higher RbF source temperature results in a higher Rb content in the device as shown in Section 3.2). The sample treated without any RbF PDT does not show any sign of blocking within the investigated temperature range (see Figure S3a, Supporting Information). In contrast to the injection current, no barrier for the extraction of charge carriers is observed independent of the Rb content.

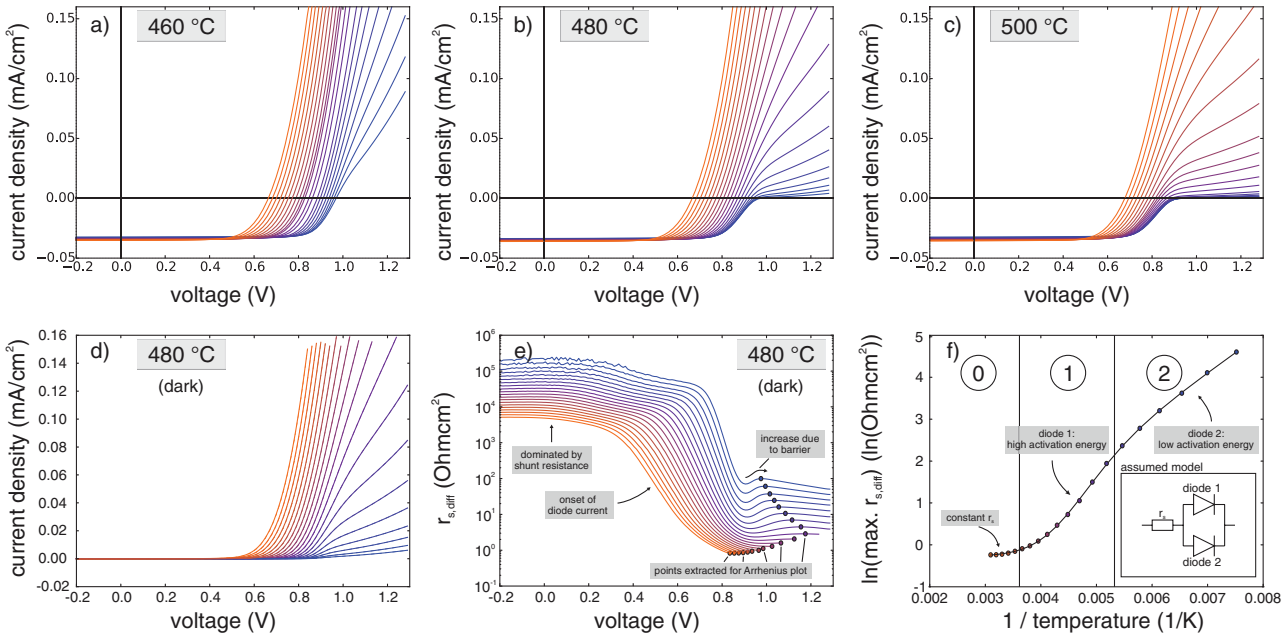

Figure 4. Evolution of the temperature-dependent (300–90 K) *I–V* behavior for an increasing Rb amount due to RbF PDT.

The quantification of the blocking is performed for the dark curves due to two reasons. First, any contribution due to voltage-dependent carrier collection can be neglected. Second, the results will be compared with data obtained from admittance spectroscopy, which is acquired in the dark as well. Dark IVT curves for the sample from a 480 °C source temperature are shown in Figure 4d. To get a value for the current blocking, the differential series resistance $r_{s,diff}$ is calculated from the *I–V* curves (see Equation (1) and Section 2) and plotted in Figure 4e. The high values of $r_{s,diff}$ in reversed and moderate forward bias above 10^3 Ohm cm^2 represent the shunt resistance of the device. For higher bias voltages, the diode current sets in, and a strong decrease of the differential series resistance is observed. The shape of $r_{s,diff}$ for even higher forward bias voltages is dependent on temperature. For high temperatures, $r_{s,diff}$ levels off, which represents the ohmic series resistance. In contrast, at low temperatures, the differential series resistance increases again due to a barrier, which limits the current transport. Extracted values for the differential series resistance are plotted in an Arrhenius diagram in Figure 4f. For high temperatures, the leveled-off values are taken, while for low temperatures, the local maximum value in high forward bias is determined (indicated by solid circles in Figure 4e) (see also Section 2). In the ongoing manuscript, the term differential series resistance will be used to refer to the extracted values as shown in Figure 4e. In the Arrhenius diagram in Figure 4f, three regimes for the differential series resistance are observed (circled numbers). Region 0 represents the ohmic series resistance and is rather constant. Region 1 is observed for slightly decreased temperatures and shows a straight line indicating a thermally activated series resistance. The slope of that straight line is proportional to the activation energy. For even lower temperatures, a change of the slope is observed, i.e., a change in the activation energy, which is represented by region 2. In particular, the slope decreases in region 2 indicating a smaller activation energy. These three regions are generally observed in all characterized devices (see Figure S4, Supporting Information). Only region 0 is not observed in devices, where the thermally activated series resistance from region 1 already dominates at room temperature (see, for instance, the curve annotated "H_2O" in Figure S4c in the Supporting Information).

As the two different thermally activated regions (region 1 and region 2) are observed for all devices, we assume two different paths in parallel for the current, which are represented by the two blocking diodes in the inset of Figure 4f. A series connection of the blocking diodes is not possible as the higher activation energy is observed at higher temperatures and thus would dominate also at lower temperatures. Additionally to the two blocking diodes, a resistance in series is added to the model (region 0). The final expression for the differential series resistance can then be written as

$$r_{s,diff} = r_s + \frac{R_{d1} + R_{d2}}{R_{d1} R_{d2}} \tag{2}$$

where R_{d1} and R_{d2} represent the resistance due to the diode 1 and diode 2, respectively (see inset of Figure 4f), and r_s the ohmic series resistance. $R_{d1/2}$ can be written as

$$R_{d1/2} = p_{1/2} \exp\left(\frac{E_{A1/2}}{kT}\right) \tag{3}$$

$E_{A1/2}$ denotes the activation energy for the (blocking) diode 1/2 and $p_{1/2}$ the prefactor describing the contribution of each diode to the blocking behavior. A physical meaning of the prefactors could be geometrical effects. For instance, a relatively high area of the device contributing to diode 1 would yield a small value of p_1. Also the thickness of the blocking layer contributes to the prefactors p_i such that a thicker layer would yield a higher prefactor.

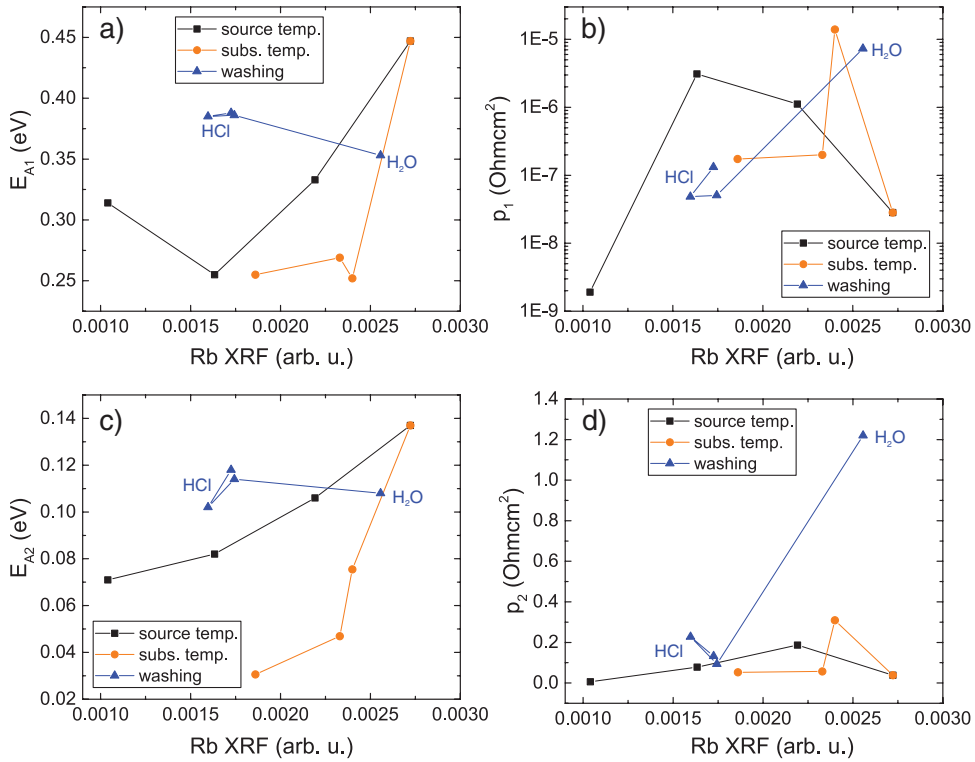

Figure 5. Fitting results from the double blocking diode model of the differential resistance. The first diode with parameters p_1 and E_{A1} represents the higher activation energy (higher slope in Figure 4f at moderate temperatures. The second diode is described by p_2 and E_{A2} representing the smaller activation energy at low temperatures.

The experimental data (solid symbols) are then fitted with the model (inset of Figure 4f) and plotted as a solid line. A good match of the fit with the experimental data is obtained for all samples (see also Figure S4, Supporting Information).

Figure 5 summarizes the fitting results of the differential series resistance. Figure 5a,b shows the parameters of the first diode at moderate temperatures, representing the higher activation energy (region 1 and stronger slope in Figure 4f), and Figure 5c,d shows the parameters of the second diode at low temperatures representing the lower activation energy (smaller slope). The parameters are plotted versus the Rb content measured by XRF to show the results for all three series. Lines connecting the data points do not have a physical meaning but serve as a guide to the eye.

Concerning the source and substrate temperature series, no clear correlation is observed for the first diode (p_1 and E_{A1}). However, an increasing activation energy of the second diode E_{A2} is observed. The prefactor does not show a clear correlation with respect to the Rb content.

In contrast, the washing series shows a different behavior. While the activation energies are rather unaffected by the washing in H_2O or HCl, a significant drop in the prefactors of p_1 and p_2 is noted. This decrease of p_1 and p_2 indicates a decreasing blocking of the diode current leading to an increased FF as shown in Figure S2 in the Supporting Information.

In a next step, admittance spectra were recorded for the samples from the three sample series. The spectra are shown in **Figure 6** for the three devices already presented in

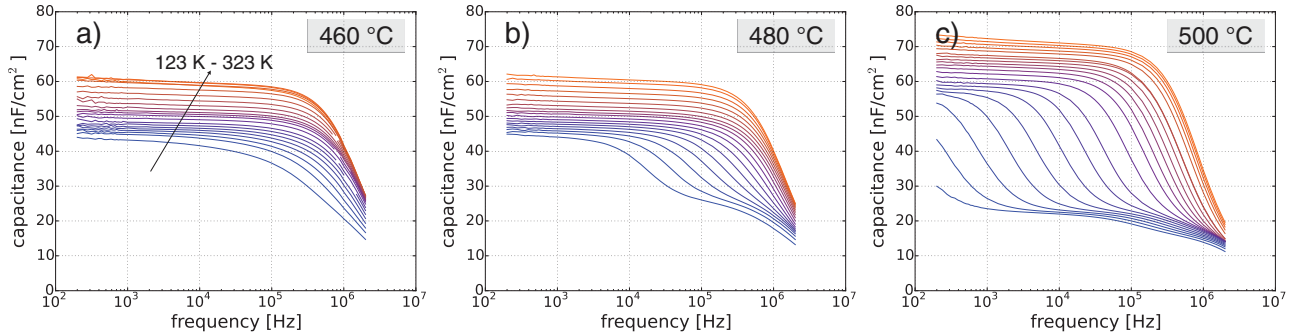

Figure 6. Admittance spectra for three devices from the source temperature series. The main impact of a higher Rb source temperature is the shift of the main capacitance step to lower temperatures.

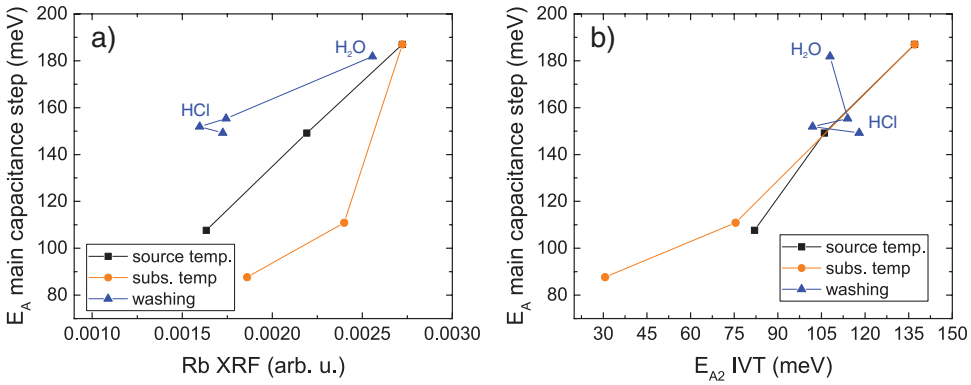

Figure 7. Activation energy of the main capacitance step with respect to the incorporated Rb content a). Correlation to the low-temperature activation energy of the differential series resistance is shown in b).

Figure 4a–c. The spectrum for the sample "no RbF" is depicted in Figure S3b in the Supporting Information. The main impact of a higher RbF source temperature (and hence an increased amount of incorporated Rb) is the shift of the main capacitance step to lower temperatures. Werner et al. investigated a large set of samples with various PDTs and showed that the main capacitance step has the same origin independent of the alkaline PDT and is consistent with the capacitance step labeled "N1."[27] To extract the drop in capacitance and the activation energy of the capacitance step, the fitting method proposed by Weiss et al. is applied to the capacitance spectra.[28] The activation energies of the main capacitance step show a good correlation to the incorporated Rb amount as depicted in **Figure 7**a. Consequently, a good correlation to the low-temperature activation energy from the differential resistance is obtained as represented in Figure 7b. Similar to the results from the differential series resistance as shown in Figure 5, the activation energies do not change strongly when washing either in H_2O or HCl.

4. Discussion

As shown in Figure 7b, a good correlation between the activation energies obtained from admittance spectroscopy and the differential series resistance is obtained. This fact points to a barrier responsible for the drop in capacitance with respect to frequency (and temperature). A barrier either at the front[29] or at the back[20] contact should give a drop in capacitance as soon as the transport over the barrier cannot follow the ac modulation. The width of the barrier w_b can then be calculated from the drop in capacitance by

$$w_b = \epsilon_0 \epsilon_R \left(\frac{1}{C_{hf}} - \frac{1}{C_{lf}} \right) \quad (4)$$

where C_{hf} and C_{lf} are the high and low frequency capacitance values of the capacitance step, respectively.[20,29] ε_0 is the vacuum permittivity and ε_R the dielectric constant of the barrier layer. For the calculations of the barrier width w_b, the dielectric constant is assumed to be $\varepsilon_R = 10$. Note that the barrier width scales linearly with ε_R. The calculated barrier width for all three-sample series is shown in **Figure 8**. Increasing the incorporated Rb amount by increasing either the source temperature or substrate temperature during the PDT results in an increased width of the barrier. This increase in the barrier width correlates with an increased activation energy of the barrier as shown in Figure 7.

Avancini et al. investigated the surface layer of a CIGS absorber layer treated with a RbF PDT.[25] It was found that similar to a KF PDT, a surface layer forms.[5–9,26,30] Additionally, as presented here for a RbF PDT, with the introduction of a KF PDT, a blocking of the diode current was observed.[15] Recently, Malitckaya et al. calculated the bandgap energies of $AlkInSe_2$ (Alk = Li, Na, K, Rb, Cs) secondary phases, which are expected to segregate on the surface of the CIGS absorber for K, Rb, and Cs.[31] It was found that $KInSe_2$ and $RbInSe_2$ both have a bandgap of ≈2.5 eV. A surface bandgap widening was observed after a KF PDT also experimentally.[8,9] These results hint to the fact that similar to a KF PDT, a RbF PDT introduces a surface layer, which might be responsible for the blocking of the diode current. That Rb-containing surface layer is subsequently called RIS layer. It has to be noted that only a blocking for the diode current is observed but not for the photo current (see Figure 4).

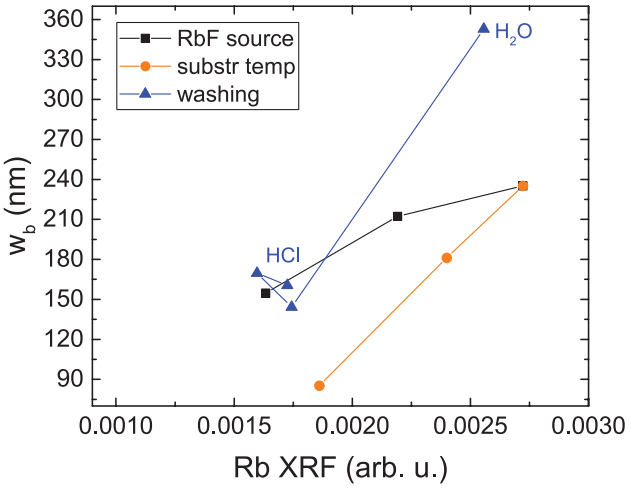

Figure 8. Calculated barrier width from the capacitance step shown in Figure 6 according to Equation (4).

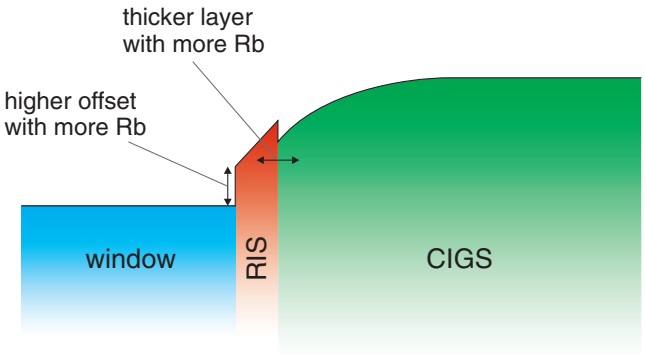

Figure 9. Schematic of the conduction band explaining the barrier behavior based on IVT and admittance measurements.

In the next step, a physical model is proposed based on the characterization results obtained from IVT and admittance measurements (see Section 3.3). For the following discussion, only the second diode is considered, which shows a good correlation between the activation energy and the amount of Rb added during the PDT as well as a good correlation between IVT and admittance measurements (see Figure 7). Since only one diode is discussed, a 1D model is sufficient as depicted in **Figure 9**. The simplified model consists of only three layers: the CIGS absorber, the Rb-containing RIS surface layer, and the window layer. The window layer in that sketch includes the Al:ZnO, i:ZnO, and the CdS layers. The barrier in that model is located at the window/RIS interface due to a conduction band offset.

First, with a higher amount of Rb, a thicker barrier layer is determined (see Figure 8). A thicker layer would also cause a stronger blocking and thus a higher value of the prefactor p_2. That behavior of p_2 can be grasped from the source temperature series but not for the substrate temperature series (see Figure 5d). However, other geometrical effects might influence p_2 as, for instance, the area covered by the layer responsible for the blocking of diode 2.

Additionally to a thicker blocking layer, a higher activation energy for the injection current is measured by IVT as well as admittance spectroscopy. The model presented in Figure 9 assumes this barrier to originate from a conduction band offset ΔE_C at the window/RIS layer. An increasing ΔE_C could result from an upward shift of the conduction band (of the RIS layer) as well as from interface dipoles.[32] Both effects might result from a different composition of the surface layer[25] due to modifications of the RbF PDT (*source temperature* or *substrate temperature series*). It needs to be stressed that IVT and admittance measurements were performed on completed devices. Thus, the influence of the CdS growth on the surface layer[33] and hence the barrier formation is not excluded.

Interestingly, a wash in HCl instead of H_2O (sample series *washing*) decreases the barrier width as presented in Figure 8. A possible reason might be the thinning of the Rb-induced surface layer. Apparently, the surface layer thinning by HCl is limited to a minimal thickness and does not proceed with longer etching times. Independent of the etching time, the calculated barrier width is the same (Figure 8). Figure 10b shows a scanning electron microscopy (SEM) micrograph of the surface layer after washing in HCl. While the surface patterning is less pronounced compared with a H_2O wash (**Figure 10**a), it does not disappear and can still be observed in the SEM micrograph in line with the quantification of the barrier width by admittance spectroscopy (Figure 8). The thinning of the barrier might then also be the reason for the reduced blocking of the diode current as indicated by the parameters p_1 and p_2 in Figure 5 leading to an increased FF.

The activation energy however does not show a change after a HCl etch compared with the H_2O washing. Thus, either the upward shift of the conduction band (or the bandgap) or the dipoles forming at the surface with the CdS layer do not change when thinning the surface layer.

However, experimentally not only one blocking barrier was observed, but two blocking diodes connected in parallel (see Figure 4f). As these blocking diodes are connected in parallel, we assume both of them present at the same interface (otherwise, they would be connected in series). Experimentally, a PDT with KF[5] or RbF[25] introduces a surface patterning. The surface patterning due to a RbF PDT is shown in Figure 10a and clearly indicates two different regions which might explain two different activation energies observed from the evaluation of the differential series resistance. A detailed investigation of the surface layer in the case of a RbF PDT can be found in ref. [25].

It needs to be stressed that the determined barrier width shown in Figure 8 only gives trends but no absolute values. The reason is that ε_R was assumed to be 10 for the calculation, but in reality, the value is not known for the barrier layer.

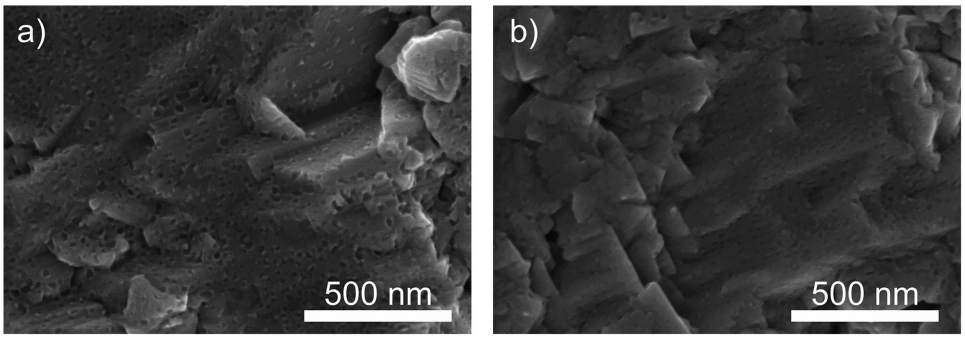

Figure 10. SEM micrographs for a CIGS absorber treated with RbF PDT. a) Shows the surface after washing in H_2O and b) after HCl wash. Figure taken from ref. [25].

5. Conclusion

A RbF PDT is employed with varying substrate and source temperature during PDT resulting in an increased incorporation of Rb into the finished solar cell devices. Mainly, the V_{OC} is improved, however, due to the formation of a barrier for the diode current, losses in the FF are observed for too much incorporated Rb.

A method for the quantification of the barrier height from IVT curves is presented and corroborated by simulation results. This method allows the quantification of the barrier heights for injection current in far forward bias from experimental IVT curves of RbF postdeposition-treated CIGS-based solar cells. Two conduction paths connected in parallel with different activation energies are observed. The surface patterning of the RbF PDT as similarly observed with a KF PDT is proposed as a possible origin.

The lower activation energy is compared with the activation energy of the capacitance step generally labeled "N1" measured by admittance spectroscopy. A good correlation of the activation energies strengthens the assumption for the capacitance step to be due to a barrier. In particular, for the samples investigated here, it could be shown that the barrier forms due to the introduction of Rb via the PDT.

Interpreting the capacitance step to be due to a barrier, the thickness of the barrier can be calculated, which increases with higher substrate or RbF source temperature during the PDT of fixed time. Etching the absorber in HCl prior to CdS buffer layer deposition results in a decreased barrier width, leading to a reduced blocking of the diode current and consequently higher FF. These results hint to the fact that the barrier is located at the front contact presumably due to a RbF PDT-induced surface layer.

6. Experimental Section

CIGS absorber layers were grown by a low-temperature multistage coevaporation process onto a Mo/SiO_2/soda lime glass substrate as detailed elsewhere.[34] Na was added in situ as a PDT after the CIGS growth. An additional in situ RbF PDT was carried out similar to the previously reported KF PDT.[4] In order to control the amount of RbF added during the PDT, the RbF source temperature (460 to 550 °C) or the substrate temperature (220 to 250 °C) was varied. The time for the RbF PDT was fixed to 20 min. The absorbers were subsequently washed with H_2O to remove residual NaF and RbF from the surface of the absorber. A CdS buffer layer was deposited by a chemical bath deposition with a subsequent air annealing for 3 min at 180 °C. It is noted that the CdS deposition time was reduced for samples treated with a RbF PDT without losing V_{OC} or FF (similar as for a KF PDT[4]) resulting in a reduction of the CdS thickness from roughly 40 to 20 nm. The i:ZnO/Al:ZnO window layers were deposited by rf-sputtering and Ni/Al grids by e-beam evaporation. No ARC was applied for the samples investigated here. Two sets of sample series were fabricated and characterized with the baseline described above and a third series with a small deviation from that. For the first sample series, the RbF source temperature was varied during the RbF PDT and was called "source temperature." For the second series, the substrate temperature was varied and was called "substrate temperature." The last series resulted from different washing procedures prior to the CdS deposition and thus was called "washing." Instead of the H_2O washing, the samples were etched in 10% HCl for different amounts of time. The RbF source and substrate temperature for this sample series had been set to 520 and 250 °C, respectively, targeting a rather high RbF amount. A summary of the sample series is presented in **Table 1**.

Table 1. Summary of the characterized sample series. The variable parameter is indicated by the series name. The fixed parameters are indicated in the row of the fixed parameters. Temperatures T_{sub} and T_{source} correspond to the substrate and RbF source temperature during the RbF PDT, respectively. The washing of H_2O or HCl stands for the washing step after RbF PDT and prior to the CdS buffer layer deposition.

Series name	Source temperature	Substrate temperature	Washing
Fixed parameters	T_{sub} = 250 °C, H_2O wash	T_{source} = 500 °C, H_2O wash	T_{sub} = 250 °C, T_{source} = 520 °C
Variable parameter	460 °C	220 °C	1 min H_2O
	480 °C	230 °C	20 s HCl
	490 °C	240 °C	1 min HCl
	500 °C	250 °C	5 min HCl
	550 °C		

A reference sample without a RbF PDT was taken for comparison and was labeled "no RbF." The absorber only received the in situ NaF PDT and a thicker CdS buffer layer as mentioned above.

Finished devices were characterized by current–voltage (*I–V*) analysis at 25 °C in a four-probe configuration with a simulated AM1.5G spectrum in an ABA-class solar simulator. Temperature-dependent capacitance and *I–V* measurements were carried out in a home-built liquid nitrogen cooled cryostat. Illumination was provided by a halogen lamp for the *I–V* measurements. Capacitance frequency measurements were carried out with a level voltage of 30 mV at 0 V bias in the dark and in a frequency range of 200 Hz to 2 MHz.

Integral composition was determined by XRF spectroscopy in a home-built setup. SEM imaging was performed on Pt-coated surfaces (≈1 nm thickness) using a Hitachi S-4800 SEM with 5 kV acceleration voltage at a working distance of 4 mm.

SIMS depth profiling was performed using a ToF-SIMS^5 unit by ION-TOF. The primary ion source was Bi+ with an acceleration voltage of 25 kV and a current of 1 pA, probing a 100 × 100 μm^2 area. O_2+ was used as a secondary ion source for depth profiling with an acceleration voltage of 2 kV and a current of 400 nA, sputtering over a 300 × 300 μm^2 area.

Dark current voltage simulations were carried out using Sentaurus TCAD. The bandgap grading was implemented by dividing the CIGS absorber into 25 regions and assigning each region a certain bandgap and electron affinity. Subsequently, these values are linearly interpolated between these 25 regions. To circumvent convergence problems at low temperatures, a constant carrier generation rate of 10^8 cm^{-3} s^{-1} was set in the CdS buffer layer. The current density resulting from the constant carrier generation in the CdS was negligible compared with the diode current considering that the CdS thickness was in the order of tens of nm.

Supporting Information

Supporting Information is available from Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

admittance spectroscopy, CIGS, postdeposition treatment, Rb transport barrier

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[1] R. Kamada, T. Yagioka, S. Adachi, A. Handa, K. F. Tai, T. Kato, H. Sugimoto, in *IEEE Photovoltaic Spec. Conf.*, 43rd., Portland, OR, USA, June **2016**.
[2] P. Reinhard, F. Pianezzi, B. Bissig, A. Chirilă, P. Blösch, S. Nishiwaki, S. Buecheler, A. N. Tiwari, *IEEE J. Photovolt.* **2015**, *5*, 656.
[3] P. Jackson, R. Wuerz, D. Hariskos, E. Lotter, W. Witte, M. Powalla, *Phys. Status Solidi RRL* **2016**, *10*, 583.
[4] A. Chirilă, P. Reinhard, F. Pianezzi, P. Bloesch, A. R. Uhl, C. Fella, L. Kranz, D. Keller, C. Gretener, H. Hagendorfer, D. Jaeger, R. Erni, S. Nishiwaki, S. Buecheler, A. N. Tiwari, *Nat. Mater.* **2013**, *12*, 1107.
[5] P. Reinhard, B. Bissig, F. Pianezzi, H. Hagendorfer, G. Sozzi, R. Menozzi, C. Gretener, S. Nishiwaki, S. Buecheler, A. N. Tiwari, *Nano Lett.* **2015**, *15*, 3334.
[6] T. Lepetit, S. Harel, L. Arzel, G. Ouvrard, N. Barreau, *IEEE J. Photovolt.* **2016**, *6*, 1316.
[7] A. Laemmle, R. Wuerz, M. Powalla, *Thin Solid Films* **2015**, *582*, 27.
[8] E. Handick, P. Reinhard, J.-H. Alsmeier, L. Köhler, F. Pianezzi, S. Krause, M. Gorgoi, E. Ikenaga, N. Koch, R. G. Wilks, S. Buecheler, A. N. Tiwari, M. Bär, *ACS Appl. Mater. Interfaces* **2015**, *7*, 27414.
[9] P. Pistor, D. Greiner, C. A. Kaufmann, S. Brunken, M. Gorgoi, A. Steigert, W. Calvet, I. Lauermann, R. Klenk, T. Unold, M.-C. Lux-Steiner, *Appl. Phys. Lett.* **2014**, *105*, 063901.
[10] R. Scheer, *J. Appl. Phys.* **2009**, *105*, 104505.
[11] N. Nicoara, T. Lepetit, L. Arzel, S. Harel, N. Barreau, S. Sadewasser, *Sci. Rep.* **2017**, *7*, 41361.
[12] S. A. Jensen, S. Glynn, A. Kanevce, P. Dippo, J. V. Li, D. H. Levi, D. Kuciauskas, *J. Appl. Phys.* **2016**, *120*.
[13] J. K. Larsen, S. Y. Li, J. J. S. Scragg, Y. Ren, C. Hägglund, M. D. Heinemann, S. Kretzschmar, T. Unold, C. Platzer-Björkman, *J. Appl. Phys.* **2015**, *118*.
[14] M. H. Wolter, B. Bissig, P. Reinhard, S. Buecheler, P. Jackson, S. Siebentritt, *Phys. Status Solidi C* **2017**.
[15] F. Pianezzi, P. Reinhard, A. Chirilă, B. Bissig, S. Nishiwaki, S. Buecheler, A. N. Tiwari, *Phys. Chem. Chem. Phys.* **2014**, *16*, 8843.
[16] J. M. Raguse, C. P. Muzzillo, J. R. Sites, L. Mansfield, *IEEE J. Photovolt.* **2017**, *7*, 303.
[17] I. Khatri, H. Fukai, H. Yamaguchi, M. Sugiyama, T. Nakada, *Sol. Energy Mater. Sol. Cells* **2016**, *155*, 280.
[18] J. T. Heath, J. D. Cohen, W. N. Shafarman, *J. Appl. Phys.* **2004**, *95*, 1000.
[19] R. Herberholz, M. Igalson, H. W. Schock, *J. Appl. Phys.* **1998**, *83*, 318.
[20] T. Eisenbarth, T. Unold, R. Caballero, C. A. Kaufmann, H.-W. Schock, *J. Appl. Phys.* **2010**, *107*, 034509.
[21] M. Igalson, A. Urbaniak, M. Edoff, *Thin Solid Films* **2009**, *517*, 2153.
[22] M. Igalson, A. Urbaniak, K. Macielak, M. Tomassini, N. Barreau, S. Spiering, in *Conf. Rec. IEEE Photovoltaic Spec. Conf.*, Seattle, WA, USA, June **2011**.
[23] A. Niemegeers, M. Burgelman, *J. Appl. Phys.* **1997**, *81*, 2881.
[24] R. Scheer, H. W. Schock, *Chalcogenide Photovoltaics: Physics, Technologies, and Thin Film Devices* **2011**.
[25] S. Nishiwaki, T. Feurer, B. Bissig, E. Avancini, R. Carron, S. Buecheler, A. N. Tiwari, *Thin Solid Films*, **2016**, *633*, 18.
[26] E. Avancini, R. Carron, T. P. Weiss, C. Andres, M. Bürki, C. Schreiner, R. Figi, Y. E. Romanyuk, S. Buecheler, A. N. Tiwari, *Chem. Mater.* **2015**, *27*, 5755.
[27] P. Reinhard, B. Bissig, F. Pianezzi, E. Avancini, H. Hagendorfer, D. Keller, P. Fuchs, M. Döbli, C. Vigo, P. Crivelli, S. Nishiwaki, S. Buecheler, A. N. Tiwari,*Chemistry of Materials*, **2015**, *27*, 5755.
[28] F. Werner, M. H. Wolter, S. Siebentritt, G. Sozzi, S. Di Napoli, R. Menozzi, P. Jackson, W. Witte, *IEEE J. Photovolt.* **2014**, *4*, 1665.
[29] T. P. Weiss, A. Redinger, D. Regesch, M. Mousel, S. Siebentritt, *Prog. Photovoltaics* **1998**, *6*, 407.
[30] A. Niemegeers, M. Burgelman, R. Herberholz, U. Rau, D. Hariskos, H. W. Schock, *ACS Appl. Mater. Interfaces* **2017**, *9*, 3581.
[31] E. Handick, P. Reinhard, R. G. Wilks, F. Pianezzi, T. Kunze, D. Kreikemeyer-Lorenzo, L. Weinhardt, M. Blum, W. Yang, M. Gorgoi, E. Ikenaga, D. Gerlach, S. Ueda, Y. Yamashita, T. Chikyow, C. Heske, S. Buecheler, A. N. Tiwari, M. Bär, *ACS Appl. Mater. Interfaces*, **2017**, *9*, 3581.
[32] M. Malitckaya, H.-P. Komsa, V. Havu, M. J. Puska, *Modelling of Interface Carrier Transport for Device Simulation*, Springer-Verlag, Wien GmbH **1994**.
[33] D. Schroeder, *Institut des Matériaux*, Université de Nantes(France) **2015**.
[34] T. Lepetit, *Thin Solid Films* **2016**, in press.