Fracture of Silicon: Influence of rate, positioning accuracy, FIB machining, and elevated temperatures on toughness measured by pillar indentation splitting

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Graphical Abstract

Abstract

The pillar indentation splitting test is a novel technique for assessing the fracture behavior of materials using micro-scale pillar samples. One typical limitation of this technique is the necessity of fabricating samples using focused ion beam (FIB) machining, which both creates damage to the samples and limits the number of samples which can be manufactured in a set timeframe. An alternative fabrication technique, lithography, is used here to fabricate a large number of (100)-oriented, Silicon micro-pillar samples. This allowed parametric studies of pillar splitting to be performed to study the influence of testing rate and positioning accuracy. Further, it allows the comparison of samples produced using different methods (lithography, Gallium FIB, and Xenon FIB) as a function of size. FIB damage was found to significantly increase the apparent toughness at smaller pillar sizes, but the influence diminishes to negligibility at pillar diameters $> 10 \mu\text{m}$. Lastly, the fracture behavior of Silicon was investigated as a function of temperatures up to 300°C . Apparent toughness values began increasing at 175°C due to crack blunting due to partial dislocation-mediated plasticity. At temperatures $> 250^\circ\text{C}$, the plasticity was sufficient to prevent splitting – requiring elastic-plastic fracture mechanics methods for further analysis.

Keywords: Silicon; fracture mechanisms; temperature dependence; pillar indentation; focused ion beam damage

Highlights

- To avoid error, necessary positioning accuracy is $\sim 20\%$ of pillar diameter.
- Influence of FIB damage on toughness observed to diminish by $10\mu\text{m}$ diameters.
- Increase in toughness observed at 175°C due to partial dislocation plasticity.
- Above 250°C , plasticity prevents Silicon pillars from splitting.

This document is the accepted manuscript version of the following article:
Lauener, C. M., Petho, L., Chen, M., Xiao, Y., Michler, J., & Wheeler, J. M. (2018). Fracture of silicon: influence of rate, positioning accuracy, FIB machining, and elevated temperatures on toughness measured by pillar indentation splitting. *Materials and Design*, 142, 340-349.
<http://doi.org/10.1016/j.matdes.2018.01.015>

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1 Introduction

Fracture toughness is a key materials property for the design of components for the most demanding applications. Recent advances in micromechanical testing have resulted in the development of many different geometries [1-6] for measuring fracture toughness on small length scales. This allows the more accurate design of micro-devices such as micro-electromechanical systems (MEMS). Since it is known that the size of materials can have a significant effect on the mechanical properties of materials, such as strength [7], it is important that materials properties are measured at the length scale of the application. For applications at elevated temperatures, property measurement at the operational design temperature is also important.

One small scale technique with potential for measuring toughness at the micrometer scale as a function of temperature is the “pillar indentation splitting test”, developed by Sebastiani *et al.* [8]. This technique is based on indentation with a sharp indenter on pillars produced using focused ion beam (FIB) machining with an aspect ratio (height-to-diameter) greater than 1. This allows local interrogation of materials toughness with high resolution [9, 10]. In sufficiently brittle materials, a crack nucleates underneath the indenter during loading, and at some critical instability, the crack extends out to the pillar surface. This instability was modeled using cohesive zone, finite element methods (CZ-FEM) to determine the relationship between fracture toughness, critical load for splitting, and pillar radius. The following relationship was found:

$$K_c = \gamma \frac{P_c}{R^{3/2}} \quad (1),$$

where γ is a dimensionless coefficient, P_c the critical load at failure, and R the radius of the pillar. The coefficient γ accounts for elastic and plastic properties (E/H ratio, where E represents the Young's modulus and H the hardness) of the material in question. The γ coefficient, which determines the position of the instability within the pillar diameter, is therefore material specific, and must be carefully selected for the material in question. If the appropriate γ coefficient is known, then only the critical load is required to be measured, as the crack length is then fixed by the pillar dimensions. Recently, Ghidelli *et al.* [11] extended the applicability of this technique for a range of indenter angles (centerline-to-face angles of 35.3-65.3°), allowing the accurate use of cube corner geometries which allow good *in situ* visualization during testing.

An excellent model material for investigation using this technique is Silicon. Silicon is widely used as a structural material for devices on the micro- and nanometer scale, especially in microelectromechanical systems [12, 13]. At ambient temperatures and large scales, Silicon can be considered a classic linear-elastic brittle material. However, Silicon undergoes a so-called brittle-to-ductile transition (BDT), where the fracture behavior transitions from a low-energy, brittle fracture to a relatively high-energy, ductile fracture at elevated temperatures [14]. This makes the characterization of the mechanical properties of Silicon as a function of temperature important to ensure its performance in service over a broad temperature range.

At small scales, increased amounts of dislocation-based plasticity is commonly observed in brittle materials [15]. The dislocation mechanism in Silicon in different temperature regimes has been heavily debated over the last decades [16-21]. The diamond cubic crystal structure of Silicon may be considered as two interpenetrating face centered cubic (FCC) lattices displaced by $\frac{a}{4} \langle 111 \rangle$. As in FCC structures, dislocations move on $\{111\}$ glide planes. The stacking of close-packed layers of each sub-lattice along the $\langle 111 \rangle$ direction results in two possible planes for dislocations to move: i) on the shuffle set, which corresponds to the plane between two widely spaced close-packed layers or ii) on the glide set, which corresponds to the plane between two narrowly spaced close-packed layers. At low temperatures and high stresses, the deformation of Silicon is thought to be governed by the motion of perfect shuffle dislocations. At elevated temperatures, there is a transition to the glide set plane, where dislocations dissociate into partial dislocations and consequently stacking faults are formed. For a detailed review on this still not fully understood issue, see Rabier *et al.* [22].

Previous measurements of the fracture toughness of Silicon at conventional length scales as a function of temperature revealed a sharp transition from brittle to ductile behavior within a small temperature range of only a few °C [23]. However, reported values for the BDT temperature varied between 545 to 805 °C, since the BDT temperature depends on the test method, doping concentration, strain rate and crystal orientation [23-25]. Additionally, due to a size effect the BDT temperature shifts to even lower temperatures for smaller specimen sizes [26-28].

Recently, Jaya *et al.* [29] determined the change in fracture behavior of micro-scale, single crystalline Silicon beams as a function of temperature by micro-cantilever bending. The measured fracture toughness displayed a more gradual increase for higher temperatures, rather than a sharp transition in fracture behavior as for bulk Silicon. They found two changes in fracture mechanism: the first one at intermediate temperatures (300, 400 °C) and a second one at high temperatures (500, 600 °C). In the intermediate temperature regime, the fracture behavior changed from a single catastrophic brittle fracture to a mechanism where crack branching occurred, associated with multiple load drops in the load-displacement curve. In the high temperature regime (above 500 °C), extensive crack deflection is observed, without any branching events. However, since the toughness values continued to increase up to 600 °C, without any plateau with temperature, it is thought that the BDT may be at yet higher temperatures.

In this work, this gradual increase in fracture toughness as a function of temperature on the micrometer-scale will be further investigated. This will be achieved by reducing the temperature steps between measuring points, allowing for a more accurate determination at which temperature the increase in fracture toughness occurs and related changes in dislocation mechanism happen. By using lithographically produced pillars, the limitations in the number of available samples usually imposed by FIB techniques is removed. The use of lithography Si pillars, similar to those utilized in previous work [30], also removes concerns of FIB damage [31] or Gallium embrittlement at elevated temperatures [32]. It also allows the influence of a variety of testing parameters to be investigated, which might normally be ignored. Here, the influence of testing rate, positioning accuracy, and pillar fabrication technique is investigated to determine their effect on pillar indentation splitting toughness results. Then, by combining this technique with a high temperature nano-mechanical testing system, the fracture toughness of Silicon is investigated at elevated temperatures.

2 Materials and Methods

2.1 Pillar preparation

2.1.1 Lithography process

The lithography Silicon pillars were fabricated at the Center for MicroNanoTechnology, EPFL in Lausanne, Switzerland. A Silicon wafer with (001)-orientation was coated with a 600 nm thick photoresist layer (AZ ECI 3007, MicroChemicals) by spinning at 6000 RPM. After soft baking at 100 °C, direct laser writing was used to microstructure the coated layer. By using an Alcatel AMS 200E inductively coupled plasma etcher, the pattern of the square grid of round pillars was transferred into the Silicon substrate. Before exposure, the direct laser writer was aligned with a below 1 mrad ($\sim 0.057^\circ$) precision to the primary flat of the Silicon wafer, which is aligned to the (100) plane with $< 1^\circ$ precision by the supplier. The pillar grid is therefore aligned to the (100) plane within $< 1^\circ$ precision.

Alternating etching and passivation steps were conducted in an 1800 W plasma, using SF₆ for etching and C₄F₈ for polymer passivation of the pillar sidewalls. The average etch rate was 4.75 $\mu\text{m}/\text{min}$. Cleaning steps followed to remove any remaining photoresist and organic contamination. In order to achieve smooth pillar sidewalls and remove the passivation layer, a 2 μm thick silica (SiO₂) layer was grown on/from the substrate (wet oxidation at 1000 °C). The silica grows both downwards into the bulk and upwards out of it. Upon oxidation of a bare Silicon surface, 44% of the oxide thickness will be below the original surface, and 56% will be above it.

The grown silica layer was then removed again by immersion in a buffered HF solution. This removed the constraining, passivation oxide layer observed in previous work [30]. This combination of wet oxidation combined with an HF etch leaves the purest achievable surface in the CMOS industry. Pillars were produced by this method on two separate wafers. On one wafer, which was etched to a depth of 13 μm , grids of pillars were produced with diameters of 3.5, 4 and 5 μm and aspect ratios (height-to-diameter) of 3.7, 3.25, and 2.6, respectively. On a second wafer, which was etched to a depth of 26 μm , pillars were produced with diameters of 8 and 11 μm and aspect ratios of 3.25 and 2.36, respectively.

2.1.2 Focused ion beam milling

In order to compare different pillar preparation techniques, micro-pillars with diameters of 3.5, 6 and 10 μm with an aspect ratio of ~ 3 were produced on the same (100)-oriented wafer part using both Gallium (Ga) and Xenon (Xe) FIB systems. Progressively smaller milling currents were used in multiple stages to produce the pillars. For Ga FIB, this was done using a Helios G3 (FEI, Brno, Czech Republic) instrument with an acceleration voltage of 30 kV. An initial current of 9.3 nA was used for coarse milling, then a lower current of 0.79 nA was applied to dimension the pillar close to the designed geometry. A final surface polish was performed using an 80 pA current to minimize taper and achieve the final dimension. For Xe FIB, pillars were machined using a Fera Xe plasma FIB (Tescan, Brno, Czech Republic) with currents of 100 nA and 30 nA for coarse milling and 100 pA to 1 nA for fine milling. An exact match between milling parameters between the Ga and Xe FIB milling currents was not achievable with the current systems available.

2.2 Indentation Pillar Splitting

All pillar indentation splitting tests were carried out *in situ* inside a Vega 3 (Tescan, Brno, Czech Republic) scanning electron microscope (SEM), using a modified Alemnis SEM Indenter (Alemnis AG, Thun, Switzerland). This allowed rapid, accurate positioning of the indenter above the pillars and visualization of the fracture onset. The large number of available pillars provided by the lithographic processing allows the experimental investigation of the influence of several testing parameters: testing rate, positioning accuracy, and the influence of FIB damage.

In all cases, a diamond cube corner indenter was used to perform the splitting, and a facet edge of the cube corner was kept aligned with the (010) plane of the Silicon. This was done manually, in the absence of a precision rotation stage, so the accuracy of the indenter's alignment to the (010) plane is on the order of a few degrees. This was in order to minimize any variation due to crystallographic variation of fracture toughness due to the preferred {110} and {111} cleavage planes of Silicon. For determining the critical stress intensity, K_c , from the critical load using Equation 1, a value of 0.607 was used as the γ coefficient for Silicon at ambient temperature. This is further discussed in Section 4.1.

In situ images were used to measure the diameter of each pillar tested. Since the pillars were imaged with a 20° tilt with respect to the electron beam and due to edge rounding effects in the case of FIB machined pillars, the diameter was measured from sidewall to sidewall in the upper part of the pillar, rather than on the top surface.

2.2.1 Rate dependence

To investigate the influence of rate, indentation pillar splitting was performed on pillars with a diameter of 5 μm at several different displacement rates (2, 10, and 50 nm/s), covering 1.5 orders of magnitude in variation. In testing for Sections 2.2.3 and 2.2.4, the pillars with larger diameters (6-8 and 10-11 μm) were tested using displacement rates 7 and 10 nm/s, respectively, to keep the displacement rates in proportion to the pillar heights.

2.2.2 Positioning accuracy dependence

To determine the influence of positioning accuracy, or the accuracy with which the indenter is centered over the pillar, a series of pillars were split with the indenter deliberately positioned at

offsets from the center of the pillars. This was accomplished by first centering the pillar underneath the cube corner indenter using the X-Y positioning stage of the system in conjunction with *in situ* imaging of the SEM, then the indenter was offset by increasing increments in the lateral (X-axis) direction. Pillar splitting was then performed at these offset locations at a displacement rate of 5 nm/s. Since the cube corner indenter does not have radial symmetry, an additional round of tests was performed with the indenter offset in the Y-axis direction as well. To achieve good measurement accuracy, the offset distance between the splitting indentations and the central axis of the pillars was measured after splitting using SEM imaging of the top surfaces of the pillars, rather than using the *in situ* videos. The *in situ* accuracy of positioning in the Y-axis in the SEM is always reduced, compared to the X-axis due to the 20° tilt of the sample stage with respect to the electron beam.

2.2.3 Manufacture method influence

A concern for nearly all micromechanical testing is the possible influence of damage from FIB machining on the results. The use of lithographically produced pillars allows the direct comparison of results with and without FIB damage. Furthermore, since the FIB damaged zone is expected to be localized near the surface in larger samples, it is worthwhile to investigate the influence of sample size. As stated above, pillars of 3.5, 6 and 10 μm diameters were produced using both Xe and Ga FIB machining, and a minimum of 4 pillars were tested for each case. Additionally, one set of 6 pillars with a diameter of 3.5 μm were machined using Ga FIB and subsequently annealed in vacuum at 300 °C for one hour to determine if recrystallization of the amorphized layer [33] resulted any different behavior.

2.2.4 Elevated temperature splitting

Elevated temperature testing was performed using a modified version of the Alemnis system [34] mentioned above that allows independent heating of the indenter and the sample. The thermally calibrated indenter can be used as a surface temperature probe, which allows to determine the sample surface temperature with an accuracy of 1% [35]. This enables performing temperature tuning indentation, which is an efficient way to match the temperature of the indenter with the sample surface temperature. This temperature matching procedure is important to significantly reduce thermal displacement drift due to thermal expansion. The *in situ* testing of Silicon inside a SEM is beneficial, since oxidation of Silicon during the splitting experiments should be prevented, due to the systems vacuum conditions. Pillars with a diameter of 5 μm were tested at 25, 63, 100, 125, 150, 175, 200, 225, 250, 275 and 300 °C. Pillars with a diameter of 8 μm and 11 μm were tested at 200, 250 and 300 °C. Five pillars were tested at each temperature.

3 Parametric Studies: Influence of Rate, Positioning and FIB Damage

3.1 Influence of Testing Rate

At elevated temperatures, it is well known that the brittle-ductile transition in many materials, including Silicon [36], depends on the applied strain rate. In determining the initial parameters for later elevated temperature testing of Silicon using the indentation splitting technique, it was desirable to determine if any rate dependence was observable at ambient temperatures.

In the indentation geometry, it's known [37] of a self-symmetric indenter is the displacement rate divided by the current displacement, $\dot{\epsilon} = \dot{h}/h$. Thus, for a constant displacement rate, the indentation strain rate would linearly decrease with increasing depth, so it might be expected that the final strain rate at the onset of unstable crack growth would depend on the depth of the indenter. However, in this case, the indentation strain rate, which is related to the indentation's plastic zone, is not the same as the strain rate applied at the crack tip, since the cracks extend outside the plastic zone of the indentation. This would suggest that the strains and strain rates at the crack tips will be lower than any estimate of indentation strain rate.

Figure 1 – Influence of rate on indentation splitting toughness measurements.

Since the strain rate at the crack tips is not equivalent to the indentation strain rate, and the testing system employed for pillar splitting is intrinsically displacement-controlled, the influence of rate was investigated using constant displacement rates during testing. This is preferable to a proportionally increasing loading rate ($\dot{P}/P$) or proportionally increasing displacement rate ($\dot{h}/h$), since it precludes any chance of catastrophic overloading. This prevents possible damage to the indenter and leaves the split pillar in good condition for later characterization. The influence of displacement rate on the toughness results is shown in Figure 1. This shows the critical stress intensity, K_c , to be roughly constant within the scatter of the measurements between displacement rates of 2 – 50 nm/s. Further testing in all other sections of this work are all performed within the middle of this range of displacement rates.

3.2 Influence of inaccurate indenter positioning

A significant benefit of the pillar splitting technique is that it allows *ex situ* testing. For *ex situ* testing, the accuracy of the alignment between the indenter and the microscope, together with the accuracy/precision of the positioning stages, determines the accuracy of the placement of the indenter on top of the pillar for splitting. As mentioned in Section 2.2.2, *in situ* testing allows very accurate positioning of the indenter above the pillar in the X-axis direction, but reduced accuracy in the Y-axis, due to sample tilt. Thus, it is desirable for both *in situ* and *ex situ* testing to know the influence of positioning accuracy on the results. This allows one source of error/scatter in the results to be quantified and helps determine the relative positioning accuracy necessary for a given pillar size to attain accurate results.

The variation in measured critical stress intensity, K_c , as a function of indenter positioning offset from the center of the pillar is shown in Figure 2. Two different indenters were used for this experiment. The primary investigation was performed using a room temperature indenter with a tip radius of ~ 500 nm, as used in the previous section, and the follow-up investigation was performed using a new high temperature, cube corner indenter with a tip radius of ~ 200 nm. For both indenters, within a radius of 350 nm off-center, the fracture toughness remains unchanged. However, the sharper indenter does achieve an instability at a lower stress intensity, as might be expected. At larger offset distances, the apparent fracture toughness starts to decrease. This decreasing trend continues towards a toughness of zero as the edge of the pillar is approached, as would be expected.

Figure 2 – Apparent fracture toughness as a function of distance to the center of the pillar with the offset orientation direction and the indenter tip radius noted.

As the loading is no longer axisymmetric, the radial symmetry assumed in the CZ-FEM for determining the toughness to critical load relationship (Equation 1), is no longer valid. Instead, the critical load is reduced, since the distance for one of the cracks formed from a facet edge of the indenter to traverse until it meets the pillar side surface is reduced, while the other two are increased. This can be clearly seen in Figure 3, where a pillar was split by a slightly misaligned indenter, and the transition between sub-critical and super-critical crack growth is delineated. This is seen to be independent of whether the indenter is offset along the X or Y axis in Figure 2 in both positive and negative directions, relative to the Cartesian center position of the pillar. One reason for this independence is likely the difference between the 3-fold symmetry of the cube corner geometry and the 4-fold symmetry of the pillar's crystallographic (001) orientation. Since these symmetries can never be aligned in this orientation, the influence of the crystallographic orientation on the results is limited.

Figure 3 – Secondary electron (SE) micrograph of a lithography pillar split by a slightly off-center indentation, showing the transition from sub-critical to critical crack extension.

Within a radius of 350 nm from the center of the pillars or ~14% of the pillar radius, the measured fracture toughness stayed at the same value (see Figure 2). This plateau may be due to the blunting influence of the plastic zone under the indenter causing the initial crack nucleation to be delocalized from directly underneath the indenter. Otherwise, one might expect the critical stress intensity to directly decrease as the misalignment of the indenter increases, without a plateau region. However, this plateau is useful for providing a rough guideline for the required positioning accuracy for performing this type of test.

These results suggest that to perform consistent fracture toughness measurements on brittle materials, the indenter's positioning accuracy should be at least $\sim 14\%$ of the pillar's radius, or to be more conservative, 20% of the pillar's diameter. This is consistent for both a sharp and somewhat blunt cube corner indenter. However, these values may vary with pillar diameter and test material. With these caveats, a rough rule-of-thumb guideline would be that the positioning accuracy of the system should be at least $\pm 10\%$ of the pillar diameter to be tested. For example, to accurately test the toughness of a pillar with a $10\text{ }\mu\text{m}$ diameter, the positioning accuracy of the sample stage and microscope calibration should be at least $\pm 1\text{ }\mu\text{m}$.

3.3 Comparison of lithography and FIB-machined pillars

A concern with all small scale test geometries produced by FIB machining is whether the sample is damaged by the FIB and what is the magnitude of this damage. Unfortunately, FIB is usually the only method available to make such samples, so no comparison to an undamaged sample can be made. However, with lithographically produced pillars as a reference in this case, a comparison may be made to ascertain the magnitude of the effect of FIB machining on the apparent measured toughness. The results of this comparison are presented in Figure 4.

In general, FIB machining is observed to produce an increase in the measured toughness, especially for smaller pillars. As the pillar size is increased, the results from pillars manufactured by FIB appear to converge towards the constant plateau of the lithography pillars. A simple, empirical fit of the data using an exponential decreasing function suggests that at pillar diameters greater than $10\text{ }\mu\text{m}$, it appears that results from pillars produced by either FIB or lithography should give good agreement between measurements.

The constant plateau of K_c values for the lithography pillars raises an interesting point regarding the influence of aspect ratio on the measured K_c . Since the lithography pillars with diameters from 3.5 to $5\text{ }\mu\text{m}$ all have the same height, these pillars have aspect ratios ranging from 2.6 to 3.7 . However, Figure 4 shows that the measured K_c is apparently unaffected by the variation in aspect ratio. Sebastiani's method [38] was initially developed with an aspect ratio of 1 , which allows a semicircular crack to simultaneously reach the bottom and the side wall of the pillar. Since the constraint to crack growth is provided by the side walls, not the base, a taller, higher aspect ratio pillar would be expected to behave identically to a pillar with an aspect ratio of 1 on a slightly more compliant substrate. This has been shown [38] to have a negligibly small influence on the critical load for splitting. Once the pillar reaches a sufficiently high aspect ratio for buckling to occur at the splitting load, then a change in fracture behavior would be expected. In microcompression of silicon pillars, buckling has been observed [30] at an aspect ratio of 4.2 . Since splitting is required to occur at a lower load than compressive failure of the pillar for this technique to be valid, it would be expected that buckling during indentation splitting testing would begin to occur at a higher aspect ratio than observed in compression. Thus, these results suggest that the aspect ratio range within which that indentation pillar splitting can be successfully performed now extends between 1 and ~ 4 .

Comparing the results obtained in this work to those in the literature [3, 11, 38], it is observed that values reported in the literature are somewhat higher than those measured here. The values from Jaya *et al.* [3] from 2015 (hollow diamond) appear to agree quite closely with Ga FIB and lithography results from this work. However, these measurements were acquired using a cube corner indenter, while the K_c values were calculated using the γ coefficient for a Berkovich indenter ($\gamma = 0.305$), since the γ coefficients for cube corner indenters were not yet available. Upon recalculating the K_c values using the correct γ coefficient ($\gamma = 0.606$) for the indenter used, the values can be seen in Figure 4 (solid diamond) to be significantly higher than all other results. This is possibly due to differences in sample doping level or indenter sharpness. Results from Sebastiani [38] and Ghidelli [11] are also slightly higher than observed here, but they are still within the accepted range of toughness values (0.7 - 1.3) for single crystal Silicon [39]. Again, inter-sample differences may play a role in this, or a difference in indenter sharpness. However, for directly comparable cube corner results [11], a 7% difference in γ coefficient is also seen:

Ghidelli, $\gamma = 0.660$ and here, $\gamma = 0.606$. If this difference is adjusted for, then Ghidelli's results are in good agreement with the Ga FIB results obtained here.

Figure 4 – Variation in critical stress intensity as a function of pillar size for different production methods compared to literature values [3, 11, 38] with indenter geometry (CC – Cube Corner, Berk – Berkovich) and γ coefficient given.

The source of the differences between manufacturing methods observed in Figure 4 is attributed to the resulting surface states of the pillars after fabrication. Since the lithography process was performed following a new protocol, the surfaces of the lithography pillars are near pristine with only a thin native oxide and no residual stresses. The surfaces of the pillars fabricated by FIB have a damaged, amorphized layer with a thickness of about 20-30 nm (30 kV beam) containing implanted gallium [40] in the case of Ga FIB. The fracture toughness of amorphous Silicon (1.0 MPa√m) is higher compared to single crystalline Silicon (0.7 MPa√m) [41]. Further, tensile stresses at the surface [42] and compressive stresses at the amorphous-crystalline interface are introduced [43] due to FIB milling. The higher fracture toughness of the amorphous layer and the compressive stress state at the amorphous-crystalline interface would change the critical crack length for the instability and increase the fracture toughness values of FIB milled pillars. This explains the apparent increase in fracture toughness for pillar produced by FIB.

However, the effects of the damage from Xe FIB pillar production appear to be nearly twice as severe as that from Ga FIB. This is contrary to previous investigations [44] on Ga vs. Xe FIB amorphization of Silicon, which shows that Xe produces a 40% smaller amorphized zone than Ga FIB at 30 kV acceleration voltage. Initially, rather than any difference in damage mechanism, the higher apparent toughness values from pillars made using Xe FIB were attributed to the higher taper angle (Figure 4) in the produced pillars. However, the taper angle remained constant at $\sim 5.5^\circ$ at all sizes, so the taper angle would not explain the decreasing trend with increasing pillar diameter. Instead, the increased damage for the Xe pillars is attributed to the higher ion dose received by the pillars during fine polishing at higher beam currents.

In an attempt to ascertain if the FIB damage could be ameliorated by annealing, one set of the smaller Ga FIB pillars was annealed at 300 °C for one hour. The thermal treatment should reduce influences of the FIB damage introduced into the material. During annealing the Ga migrates to the surface and the amorphous Silicon layer starts to recrystallize [33]. Wang *et al.* [45] compared as-milled FIB pillars and thermally-treated pillars in compression tests. As-milled pillars deformed in a ductile manner, whereas the thermally-treated pillars were brittle. They stated that the size-dependent BDT of Silicon originates from the confining amorphous layer of FIB-machined pillars, instead of the intrinsic property of crystalline Silicon. Similar to those results, a decrease in fracture toughness after annealing was expected. However, in this work, the thermal treatment was found to cause a negligible reduction in the measured toughness (Figure 4). Either the annealing temperature of 300 °C was insufficient to induce the recrystallization of amorphous Silicon [46] or the recrystallized Silicon also resisted crack extension.

The damage introduced during sample preparation by top-down, annular FIB milling influences the results of pillar indentation tests significantly, as the fracture toughness measurements in this

study demonstrate. This is contrary to the expectations of the developers of this technique, who presumed that effects of FIB machining on this geometry are negligible [8]. This is correct for the nucleation of the initial, sub-critical crack, but not for the critical load of the instability, where the critical crack extension to the surface occurs. We assume that pillars produced by lithography give the most accurate values for the tested Silicon sample, since both material alteration seems to be the smallest and the geometric accuracy seems to be the highest with this preparation technique. Given that annealing fails to significantly reduce the apparent K_c , it is suggested that the effects of FIB damage can be reduced by two methods: low beam currents and larger pillars. Using lower beam currents reduces the implanted ion dose, and using larger pillars reduces the relative impact of the damaged zone by making it a smaller fraction of the pillar's volume.

4 Temperature Dependence of Fracture Toughness of Silicon

4.1 Gamma Coefficient Determination

Figure 5 – The (a) Young's modulus [47, 48] and (b) Hardness [49, 50] of (100) Silicon as a function of temperature with the resulting (c) E/H ratio and (d) gamma coefficients determined using Ghidelli's relationships [11].

In order to determine the critical stress intensity, K_{c} , at elevated temperatures using the pillar indentation splitting technique, the ratio of the elastic modulus to the hardness (E/H) of the material must be known at the temperatures in question in order to calculate the correct γ coefficients for those temperatures. Since both E and H change as a function of temperature, literature values for both properties are required for the temperature range of interest. The Young's modulus for (100) Silicon is well described in literature [47, 48] for this temperature range, but a continuous description of the behaviour with temperature is necessary for generating E/H ratios at arbitrary test temperatures. To accomplish this, the two datasets were regression fitted to Wachtman's equation [51]:

$$E = E_0 - CT \exp\left(\frac{-T_0}{T}\right) \quad (2),$$

where E_0 is the Young's modulus at 0 K, C is an exponential fitting parameter, and T_0 is the elevated temperature in °C where the Young's modulus approaches a linear relationship with temperature. The fit shown in Figure 5a is for values of $E_0 = 131.9$ GPa, $C = 0.0126$, and $T_0 = -73.2$ °C.

In contrast to literature values of elastic modulus, reported hardness values [49, 50, 52, 53] show much more variation due to the pressure-induced phase transformation of Silicon that occurs underneath the indenter. This causes the hardness to plateau at the stress necessary to cause the transformation at that strain rate and indenter angle [54]. This is clearly seen in the hardness plateau observed in the data from Gridneva *et al.* [50]. This plateau is not seen in the Berkovich hardness results from Yonenaga and Suzuki [49] due to their higher loading rates, which indicates that their results are less affected by the phase transformation. In the cube corner geometry, the material underneath the indenter is not typically transformed. Instead, the transformed material is extruded out into the pile-up around the indenter [54]. Thus, it is not expected that the phase transformation will interfere with the fracture behavior with this geometry.

Table 1 – Interpolated E/H ratios from [49] and [47, 48] and the resulting [11] gamma coefficients for Silicon at elevated temperatures.

Temperature (°C)	E/H	γ
25	9.392	0.607
63	10.657	0.640
100	11.394	0.658
125	11.685	0.665
150	11.856	0.669
175	11.950	0.671
200	12.007	0.673
225	12.070	0.674
250	12.180	0.677
275	12.378	0.681
300	12.706	0.688

As the CZ-FEM models used to determine γ coefficients for pillar indentation splitting do not include phase transformations, it is preferred to use hardness values which are representative of the materials behavior in the absence of the transformation. Further, the CZ-FEM modeling was based on Berkovich hardness values and their relation to yield strength, so it is best if the hardness values used in the E/H ratio determinations are from the Berkovich indenter geometry. Thus, it was decided to use the values from Yonenaga and Suzuki [49] in this study, rather than obtaining hardness data *in situ* using the same cube corner indenter in parallel with the pillar splitting tests. The determined values of the E/H ratios and γ coefficients for the temperatures investigated are listed in Table 1.

It is worth noting the possible variation in measured K_c values that can result from the variation in hardness data from different sources. As shown in Figure 5d, the maximum deviation seen between the gamma coefficients calculated from the two literature sources is around 15%. As discussed previously in Section 3.3, the determination in gamma coefficient can result in minor variations between measured K_c by different researchers. However, larger variations or step changes in K_c values would be independent of any selection bias from gamma function calculation from smooth fits.

4.2 Fracture Behavior

Using the indentation pillar splitting method at elevated temperatures is very similar to ambient temperature measurements. The critical loads for fracture were extracted from load-displacement curves such as the representative curves shown in Figure 6. Since the indentation was performed under displacement control, when the pillars fracture by splitting a load drop occurs in the load-displacement curve, rather than the catastrophic pop-in behavior usually seen in load-control [38]. This load drop gives a clear maximum load, which allows simple quantification of the critical load at failure. In general, the shape of the load-displacement curves shown in Figure 6 remains constant with increasing temperature, with only the maximum load varying, but some slight variations in slope can be seen due to indenter positioning variation and thermal drift. Thermal drift could not be corrected in these tests due to the fracture preventing a drift hold period on unloading. Instead, drift was minimized as described in Section 2.2.4. However, thermal drift during displacement-controlled testing in this geometry can only result in an error in displacement measurements. As the load is measured using a separate load cell, it is independent of thermal drift, so thermal drift has no influence on the measured critical loads.

Figure 6 – Representative load-displacement curves at different temperatures and representative images for the different failure morphologies observed; i.e. an ideal 3-way split for temperatures up to 225 °C, cleavage-like failure from 250 °C, and failure in the lower portion of the pillar at 300 °C.

As the temperature was increased to temperatures > 200 °C, significant changes were observed in the critical loads and the crack morphology (Figure 6). From room temperature up to 250 °C, the pillars failed under the indenter by 3-way splitting. For an ideal 3-way split, three cracks starting from each corner of the indenter nucleate and finally reach the edges of the pillar. However, it was often the case that only two of the cracks reached the edges of the pillar, in the case of small positioning inaccuracies. In that case, the crack from the third corner did not quite extend to the edge of the pillar, as shown in Figure 3.

Figure 7 shows the fracture toughness measured as a function of temperature. Different fracture mechanisms (split, cleavage and fracture in the lower portion of the pillar) were observed and are indicated with different symbols. Excluding an outlier, the fracture toughness of pillars with a diameter of 5 μm measured at room temperature was 0.72 ± 0.03 MPa $\sqrt{\text{m}}$. This is in good agreement with the generally agreed value of 0.75 to 1.29 MPa $\sqrt{\text{m}}$ for {100} single crystalline Silicon [39]. The outlier at room temperature occurred due to inaccurate positioning of the indenter (see Figure 2). The toughness remained roughly constant from room temperature up to 150 °C. At 175 °C the fracture toughness increased to 0.94 ± 0.04 MPa $\text{m}^{1/2}$. This increase could

be due to the transition to a partial dislocation mechanism on the glide set at these temperatures. The dissociation of dislocations into partials leads to the formation of stacking faults [22]. This makes crack tip shielding possible and consequently results in an increase in fracture toughness. Korte *et al.* [26] also found a change in the deformation mechanism in this temperature range (at 200 °C) while performing micro-compression tests from 25 °C to 500 °C. In their study the change in the slope of the yield stress with temperature was either associated to the transition from glide to shuffle set dislocations (similar to what Rabier *et al.* [55] found for (123) Si at 350 °C) or to the onset of cracking at lower temperatures.

Figure 7 – Individual fracture toughness values acquired with the corresponding fracture mechanism indicated.

For temperatures above 250 °C, the fracture mechanism changed to a more cleavage-like morphology, whereby from one corner of the indenter no crack nucleated (Figure 6). At 225 °C, the first more cleavage-like failure was observed, whereby a single, (010)-oriented crack nucleated from the indentation. Cleavage was the dominating failure mechanism for temperatures higher than 250 °C. In this temperature range, the partial dislocation activity becomes more pronounced. This leads to a more efficient blunting of the crack tip, until it causes cleavage as from a conical indenter rather than a triangular pyramid. The blunting of the crack tip explains also the apparent increase of the fracture toughness, since the stress intensity factor is increased to propagate the crack [56].

At 300 °C, the blunting of the crack tip seems to be too pronounced to propagate the crack before the pillar fails elsewhere under the applied load. That the crack may be arrested due to crack tip blunting is also indicated by the much higher indentation depth until the pillar fractures (see Figure 6). The scattering of the data points acquired increased considerably (Figure 7). Three out of five pillars with a diameter of 5 μm (black symbols) fractured in the lower portion of the pillar and no splitting occurred. This resulted in significantly higher loads at failure (and consequently higher fracture toughness values) compared to split pillars. Due to the absence of splitting, the cohesive finite element simulations performed by Sebastiani *et al.* [11] do not apply anymore, and calculated K_c values for this temperature are invalid. Consequently, fractured and “cleaved” pillars have been excluded in the following analysis. Table 2 summarizes the critical stress intensities, K_c , measured for different pillar diameters as a function of temperature, including only measurements with valid splitting behavior.

Table 2 – Critical stress intensity values of different pillar diameters (5, 8, and 11 μm, respectively) as a function of temperature.

T [°C]	K_c (MPa√m)		
	5 μm	8 μm	11 μm
25	0.67 ± 0.11		
63	0.77 ± 0.05		

100	0.74 ± 0.08		
125	0.77 ± 0.10		
150	0.76 ± 0.07		
175	0.94 ± 0.04		
200	0.97 ± 0.05	0.97 ± 0.03	1.02 ± 0.06
225	1.14 ± 0.07		
250	1.32 ± 0.06	1.19 ± 0.06	1.26 ± 0.06
275	1.71 ± 0.15		
300	3.29 ± 0.62	1.70 ± 0.10	1.86 ± 0.32

To attempt to acquire valid splitting behavior at temperatures higher than 300 °C, pillars with larger diameters of 8 μm and 11 μm were also tested (Figure 7). These pillars were excluded from the analysis in Section 3.3, since they were manufactured on a separate wafer with a different doping state to the smaller pillars. However, at high temperatures, even the largest pillars also failed by cleavage or compressive fracture rather than splitting. Pillars with a diameter of 8 μm showed lower fracture toughness values at the same temperature compared to pillars with a diameter of 11 μm (see Figure 7). An explanation for that could be the higher aspect ratio of those pillars (~ 3.25) compared to the aspect ratio of pillars with a diameter of 5 μm (~ 2.6) and 11 μm (~ 2.4). However, no variation in toughness was seen within a similar range of aspect ratio for the smaller pillar sizes investigated. In order to acquire valid pillar indentation splitting K_c measurements where three-fold splitting occurs, in this elevated temperature range ($T > 250$ °C), it appears that significantly larger pillar diameters would be required.

4.3 Literature Comparison

The pillar indentation splitting test geometry proposed by Sebastiani *et al.* [1] was used to evaluate the fracture toughness of micrometer-sized pillars from room temperature to 300 °C. This technique allowed evaluating the fracture toughness of micrometer-sized Silicon in a reproducible manner with only small standard deviations up to temperatures of 250 °C. The combination of this technique with lithographically produced pillars to remove sample number limitations allowed much finer temperature increments of only 25 °C to be achieved. Other comparable studies used temperature steps greater than 100 °C (see Figure 8) due to the time-consuming specimen preparation by FIB. In this work, in excess of 250 pillars were tested, providing nearly an order of magnitude more data than similar studies [29, 41].

Figure 8 – Critical stress intensity values from different pillar sizes as a function of temperature in comparison to literature values from cantilever bending tests [29, 41].

Figure 8 shows a comparison to literature values for small scale K_c values. From room temperature to 150 °C, the measured fracture toughness agrees very well with the results from Hintsala *et al.* [41], where the fracture toughness was evaluated by double-cantilever, clamped beam bending experiments. In these measurements, the sample was notched using a natural crack

generated by pre-testing and re-machining the beams, so that their critical stress intensities are independent of notch radius or damage effects.

In the temperature range from 150 to 250 °C, the fracture toughness values of the present study lie in between the two literature data sets and approach to the values measured by Jaya *et al.*, who conducted single cantilever bending experiments. Single edge notched cantilever beam tests from Jaya *et al.* were produced and notched using FIB machining. This is known to impart residual stresses at the notch tip due to gallium implantation, which, in combination with the finitely sharp notch, can cause toughness values to be overestimated [57]. This may explain some of the difference between Jaya and Hintsala's results. Jaya *et al.* found indications of partial dislocation activity at 300 °C in terms of crack blunting and branching, and multiple faceted fracture surface morphology. If similar partial dislocation activity acted to prevent or delay the crack from nucleating underneath the cube corner indenters, then this would significantly increase the critical load or cause the loading case to deviate from the boundary conditions modeled in the CZ-FEM model for indentation pillar splitting. The latter is certainly the case for pillars which failed by compressive fracture, rather than splitting (Figure 7), and generated very high apparent toughness values.

Since Figure 8 only includes valid K_c values where the pillars fractured by three-fold splitting, the increasing K_c values are attributed to the effects of crack blunting and/or delayed crack nucleation by partial dislocations. This suggests that the amount of plasticity/ductility in Silicon is too large in this elevated temperature range for toughness to be measured using the pillar indentation splitting method using linear-elastic fracture mechanics. In other words, the K_c values measured using this method begin to deviate far from the intrinsic K_{Ic} values for Silicon due to the increasing contribution of plasticity which is not accounted for by this technique. Either an elastic-plastic fracture mechanics modification to this technique or a different geometry which promotes a purer state of plane strain is required to accurately measure K_c values closer to the K_{Ic} of Silicon at elevated temperatures.

4.4 Implications for Design

Silicon used in micro-electromechanical systems has reached component sizes in the micron range and is used under extreme conditions of high strain rates and elevated temperatures. The new values obtained for the fracture of toughness provide design guidelines for Silicon on the micron length scale over a significant temperature range. At near ambient temperature, the critical stress intensity for the fracture of silicon appears to be $\sim 0.7 \text{ MPa}\sqrt{\text{m}}$, in good agreement with Hintsala *et al.* [41] measurements. However, this work highlights two mechanisms for achieving significant component toughening in Silicon micro-structures: ion beam irradiation and compressive stress states at elevated temperature. Implanting damage and residual stresses via ion beam irradiation appears to allow the toughness of components to be locally increased by up to 50% on the length scale of a few microns (Figure 4). This is in agreement with observations from Norton *et al.* [57] and the differences between Hintsala's values with a pre-crack and Jaya's values with a ion-beam machined notch in Figure 8.

Much larger gains in critical stress intensity, K_c , are seen during indentation pillar splitting at elevated temperatures, $> 250 \text{ °C}$, due to crack blunting by partial dislocations. This agrees well with the enhanced compressive plasticity seen in Silicon at sub-micron scales [28] and at elevated temperatures [34, 58] in micro-pillars. Since the observed toughness increases with elevated temperatures in bending (Figure 8) are much more modest, it appears that the toughening effects of this increased plasticity may be limited to compressive loading. This suggests that designs for application within this temperature and size range may be significantly toughened by promoting compressive stress states to take advantage of the enhanced plasticity.

5 Summary and Conclusions

The pillar indentation splitting technique developed by Sebastiani *et al.* [1] was combined with lithographically produced micro-pillars to remove the limitations of FIB machining on sample

numbers. In excess of 250 pillars were tested in this work. This allowed parametric studies of pillar splitting to be performed to study the influence of testing rate, positioning accuracy, and pillar manufacturing method. By performing testing in a custom high temperature nanomechanical testing system, the toughness of Silicon was also investigated at elevated temperatures.

Parametric studies allowed significant insights into the sensitivity of the pillar indentation splitting technique to various sorts of error. By performing tests at a range of displacement rates, the technique was demonstrated to be insensitive to rate within nearly two orders of magnitude of variation. Further, the influence of indenter positioning on the results was shown to have a significant effect with off-centered indenter positioning providing significantly lower toughness values. To provide consistent and accurate measurements, the indenter's positioning accuracy should be approximately 20% of the target pillar's diameter.

The use of lithography Si pillars allowed one of the fundamental concerns of micromechanical testing, FIB damage, to be investigated for the pillar splitting technique. It had been suggested that this geometry was relatively immune to FIB damage, since the crack is nucleated inside the pillar, far from the damaged free surface. However, FIB damage was found to significantly increase the apparent toughness at smaller pillar sizes, as compared to lithography pillars. Xenon FIB machined pillars gave especially influenced results, due to the increase dose supplied by the higher minimum beam currents of the Xenon FIB. The influence of FIB damage diminishes to negligibility at pillar diameters $> 10\ \mu\text{m}$, suggesting that larger pillar diameters should be used for this test geometry.

Lastly, the fracture toughness of Silicon was investigated from room temperature to $300\ ^\circ\text{C}$. The large amount of test specimens allowed measurements with much finer temperature increments than previously. The apparent toughness remained unchanged from room temperature to $150\ ^\circ\text{C}$. At $175\ ^\circ\text{C}$, the first increase in fracture toughness was observed, and this was attributed to the onset of significant partial dislocation activity, which allows crack blunting via stacking fault formation. At higher temperatures, further partial dislocation activity leads to increasing crack tip blunting effects and a corresponding apparent increase in K_c values greatly exceeding previous literature measurements. This inconsistency suggests that the K_c values measured by this technique overestimate the true K_{Ic} values for Silicon due to plasticity contributions unaccounted for by this method. This prevented investigation of the high temperature brittle-ductile transition using this technique, however the temperature range at which shuffle-glide transition occurs in Silicon was narrowed from the wide range of $150\text{-}300\ ^\circ\text{C}$ to between $150\text{-}175\ ^\circ\text{C}$.

Acknowledgements

Sample preparation by FIB was carried out at the Scientific Center for Optical and Electron Microscopy ScopeM of ETH Zurich. M.C. and J.M.W. acknowledge the financial support through the Swiss National Science Foundation (SNSF Grant: 200021_166094).

Figure Captions

Figure 1 – Influence of rate on indentation splitting toughness measurements.

Figure 2 – Apparent fracture toughness as a function of distance to the center of the pillar with the offset orientation direction and the indenter tip radius noted.

Figure 3 – Secondary electron (SE) micrograph of a lithography pillar split by a slightly off-center indentation, showing the transition from sub-critical to critical crack extension.

Figure 4 – Variation in critical stress intensity as a function of pillar size for different production methods compared to literature values [3, 11, 37] with indenter geometry (CC – Cube Corner, Berk – Berkovich) and γ coefficient given.

Figure 5 – The (a) Young's modulus [46, 47] and (b) Hardness [48, 49] of (100) Silicon as a function of temperature with the resulting (c) E/H ratio and (d) gamma coefficients determined using Ghidelli's relationships [11].

Figure 6 – Representative load-displacement curves at different temperatures and representative images for the different failure morphologies observed; i.e. an ideal 3-way split for temperatures up to 225 °C, cleavage-like failure from 250 °C, and failure in the lower portion of the pillar at 300 °C.

Figure 7 – Individual fracture toughness values acquired with the corresponding fracture mechanism indicated.

Figure 8 – Critical stress intensity values from different pillar sizes as a function of temperature in comparison to literature values from cantilever bending tests [28, 40].

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Highlights

- To avoid error, necessary positioning accuracy is ~20% of pillar diameter.
- Influence of FIB damage on toughness observed to diminish by 10µm diameters.
- Increase in toughness observed at 175°C due to partial dislocation plasticity.
- Above 250°C, plasticity prevents Silicon pillars from splitting.

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