Supporting Information

Contact engineering of single core/shell SiC/SiO_2 nanowire memory unit with high current tolerance using focused femtosecond laser irradiation

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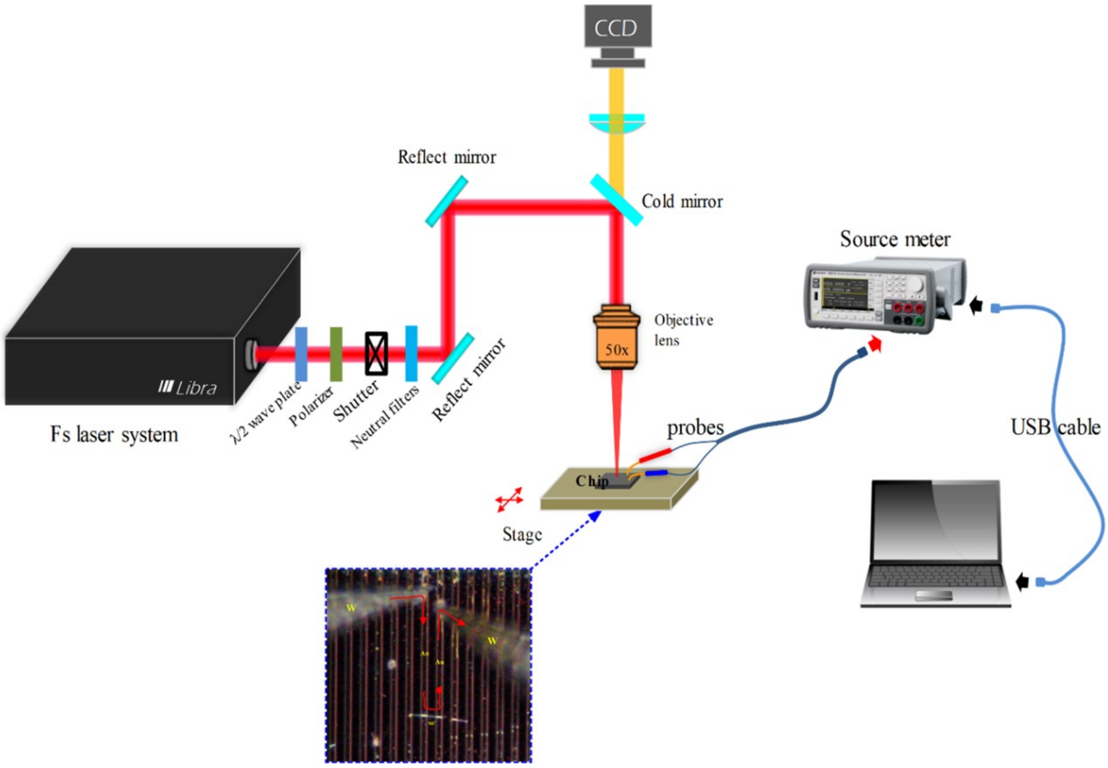

Figure S1. Schematic of the experimental set up. The fs laser beam is attenuated before entering the optical system. Using optical microscopy, the laser beam is further focused and directed to the selected points in the SiC-Au circuit. After laser irradiation, the Au electrodes were connected with two (W) probes, which are implemented in a computer controlled electrical measurement platform.

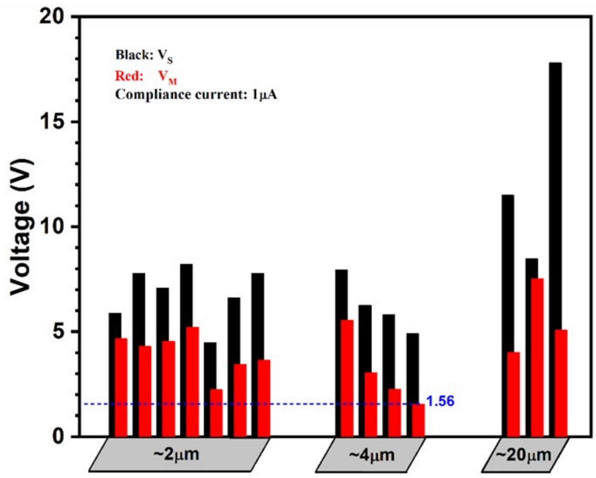

Figure S2. Statistical results of 'write' (V_S) and 'maintain' (V_M) voltages in SiC-Au circuits (before laser processing) having different bridge lengths. The difference between 'write' and 'maintain' voltages is more stable when the nanowire bridge is shorter. A low 'maintain' voltage is possible for a SiC-Au circuit when the bridging length is < 4 μm.

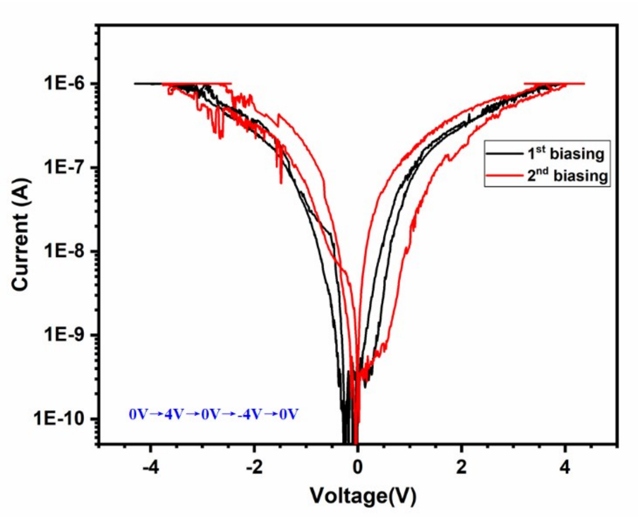

Figure S3. Current response of SiC-Au circuit under programmed voltage biasing cycles.

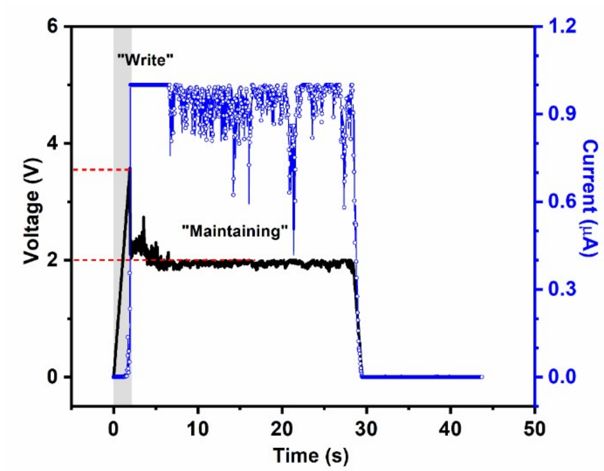

Figure S4. Current response of the 2 μm SiC-Au circuit (before laser processing) under a programmed voltage bias. The 'write' process is completed rapidly in this short-bridged structure.

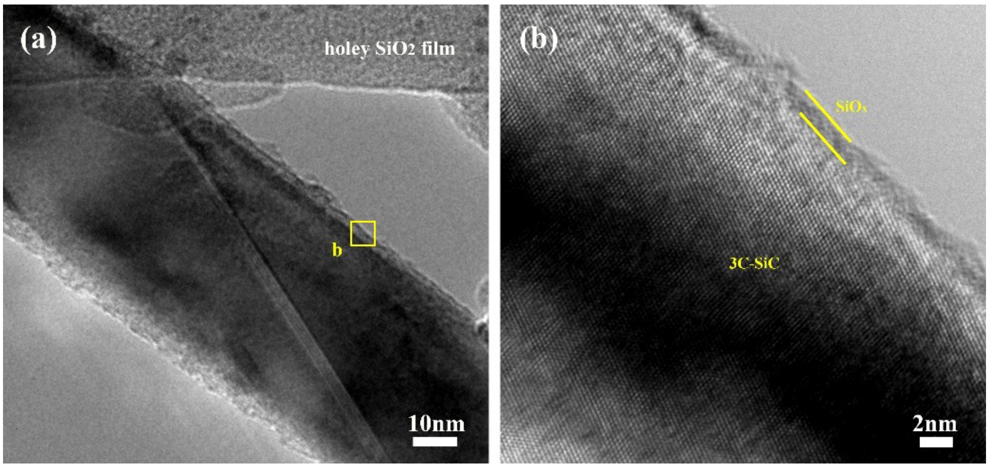

Figure S5. (a) TEM image of a core/shell SiC/SiO_2 nanowire after fs laser irradiation. (b) Magnified TEM image at the edge of nanowire. The oxide thickness is reduced to ~ 1.1 nm after irradiation. Laser fluence: 20 mJ/cm^2. Duration: 5 s.

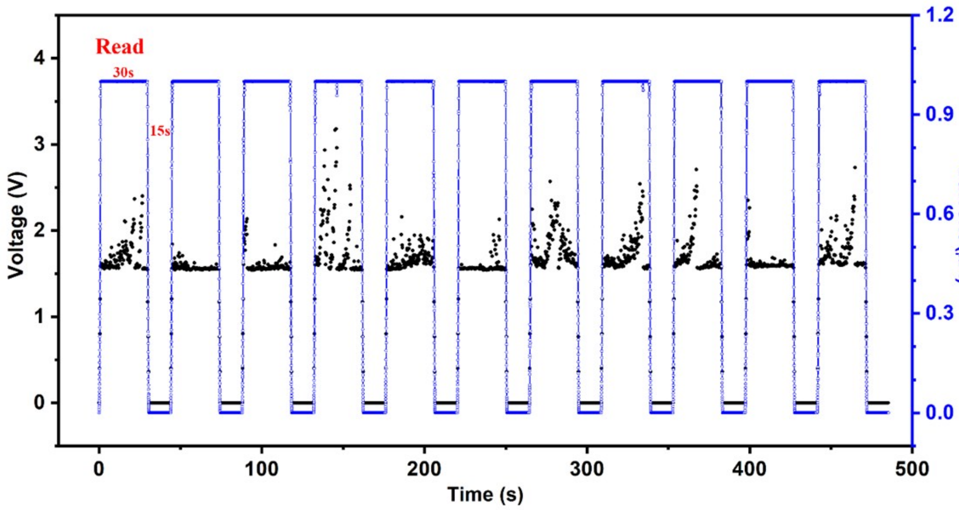

Figure S6. Consecutive 'read' processes in a SiC-Au circuit. The bias is removed for 15 s after each read operation. The read time is 30 s.

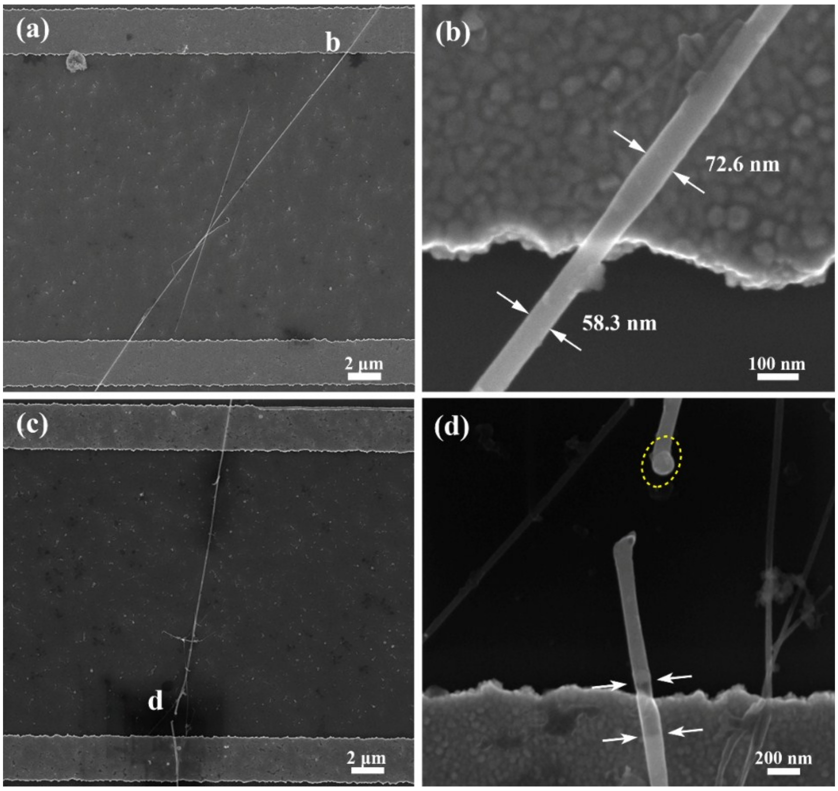

Figure S7. SEM images of electrically degraded nanowire-electrode circuits. Nanowire length (diameter) of the bridging part in (a): 21.1 μm (72.6 nm) and (c): 16.9 μm (107 nm). (b) and (d) are magnified images at locations in (a) and (c), respectively. After biasing, the nanowire circuit is still intact, while the nanowire bridge is thinned from 72.6 nm to 58.3 nm. The ends of the nanowire are melted on each side of the gap when the nanowire is broken. After breakage, segments of the nanowire appear with different image contrast (arrows in (d)), indicating that the composition of the nanowire has been changed in this region.

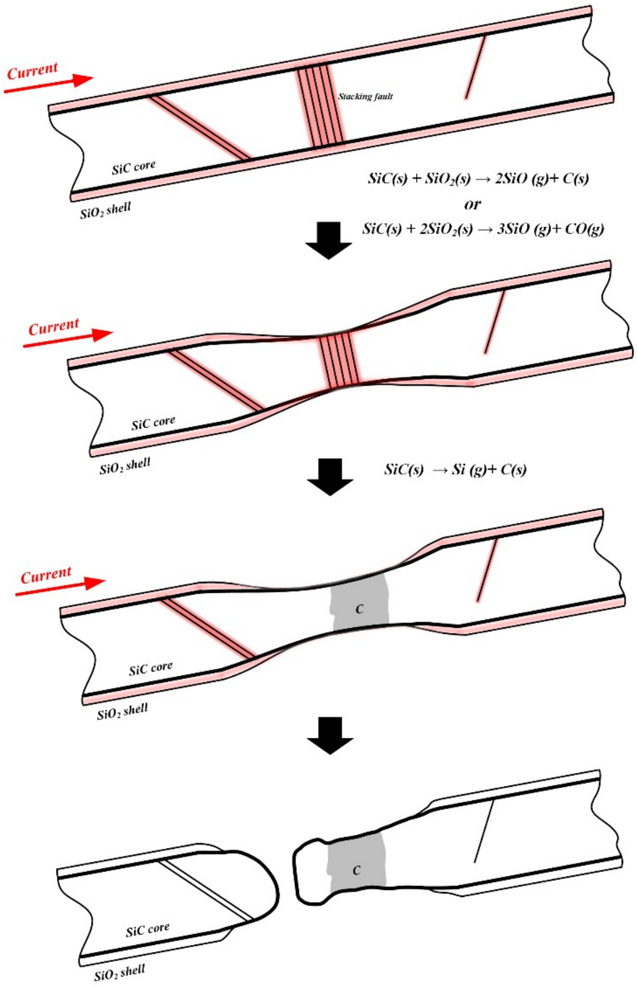

Figure S8. Schematic of the electrical breakage process in a SiC-Au circuit passing a high current. Due to the highly defective SiC core, the degradation due to thermal heating will occur preferentially at local high temperature sites. The first step involves a chemical reaction between the SiC core and the SiO_2 shell that results in the thinning of SiO_2 and the generation of C. Following this, the current density is highest in the shaded region of the stacking faults and the SiC core can dissociate to form graphite, graphene or carbon nanotubes. Further joule heating damages the oxide shell and increases the resistance so that the current drops (point A in Figure 7a). The increasing temperature in the SiC core causes the structure to melt and separate, forming a gap (point B in Figure 7a)