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Enhanced Assembly of Ag Nanoparticles for Surface-Independent Fabrication of Conductive Patterns

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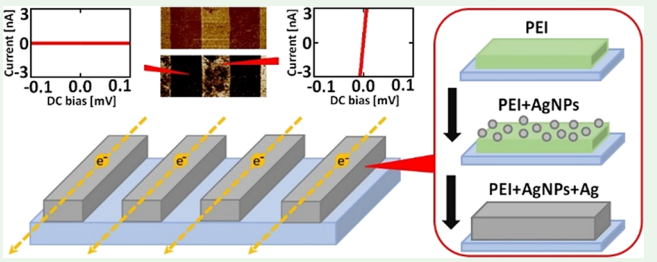
ABSTRACT: Polymer stamping is a reliable and cost-effective method for producing charged patterned surfaces. However, charge stability is limited, and they discharge steadily while immersed in polar solvents. Here, we applied polyelectrolytes as the stamping medium to increase this stability. Charged line patterns were fabricated by pressing a polydimethylsiloxane (PDMS) stamp covered with a polyethylenimine (PEI) solution against silicon, glass, or polystyrene. Then, the substrate was immersed in a solution of oppositely charged silver nanoparticles. Finally, silver crystallization on the deposited nanoparticle agglomerates was performed to homogenize the conductive surface. Fabricated structures were characterized by conductive AFM, SEM, and electrical measurements. Simulations of the electric field above the pattern and electrostatic deposition of nanoparticles were performed. The presented method allows for the production of high-resolution microstructures composed of parallel 45 mm paths with a width of 10 μm and a thickness below 100 nm. A conductivity of 10^4 S/m is high enough to keep a commercial LED on.



KEYWORDS: *nanoparticles, polyelectrolytes, conductivity, controlled assembly, surface patterning*

INTRODUCTION

Nowadays, we are surrounded by electronics. The number of sensors, wireless systems, home appliances, or "smart" devices around us is growing each year.[1,2] Most of these devices fall under modern buzzwords, such as "Industry 4.0", "wearable electronics", and "Internet of Things". However, irrespective of their names and scope, each of these technologies requires precise, fast, cheap, and reproducible implementation methods. In the case of the industrial production of advanced modern electronics (e.g., microprocessors), large-area functionalization with nanometer resolution is widely used.[3] The typical processing and replication techniques require photolithographic methods or metal target sputtering, followed by chemical dissolution of photoresists—in total, substrate-, time-, and resource-consuming, step-by-step assembly.[4] On the other hand, fast prototyping and the production of other, less complicated electronic circuits can be done at micrometer resolution,[5] which brings many benefits: from the acceleration of the production process to freedom of creativity for in-house inventors.

Taking into account future high-throughput production, the processes called replica molding should be considered.[6−9] Stamping of bare polymeric stamps on insulating substrates leads to the generation of both radicals and static charges—a process named contact electrification.[10] The radicals can act as reaction centers,[11] and charges stabilize their longevity, but eventually are doomed to decay within hours, especially while immersed in polar solvents. Polymeric stamps are also used for stamping thin films of molecular or macromolecular materials, leading to a more permanent surface functionalization. The latter often exhibits different properties and performance from those of the parent compound. In particular, when surface-grafted polymers, layers,[12−15] and brushes[16−20] serve as a matrix, they may provide good control of structure, thickness, or mechanical properties of the whole composite. The stamped film usually needs enhancement to achieve additional functionalities. This can be easily accomplished by covering the surface with functionalized nanoparticles with unique properties. These include electric, optoelectronic, plasmonic,[21] magnetic,[22] catalytic,[23] and higher order of complexity intrinsic functions, such as synaptic-like behavior and information processing.[24] To use their assemblies in displays, photovoltaic devices, sensors, microreactors, or processing units, one must first find easy-to-use protocols for nanoparticle patterning on different substrates. Several strategies have been reported so

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far. Most of them are based on self-assembly driven by multiple forces[25−27] contributing to the implementation of 2D and 3D thin-layer devices[28,29] on either rigid or flexible substrates.[30−35] Others can rely on oxidation—as for gold nanoparticles with thiol ligands, for which aggregation is induced by UV-light exposure.[36]

Direct nanoparticle transfer printing is used to produce LED displays[37] or patterned surfaces with gold nanoparticles.[38] The same procedure can be applied to both non-functionalized nanoparticles and functionalized ligand-based nanoparticles.

Here, we propose a three-step patterning technique that combines several methodologies—soft lithography, polyelectrolyte layer assembly, and nanoparticle structure assembly. Together, they yield conductive silver patterns in a reliable and scalable manner. In the first step, the polymeric stamp, covered in the polyelectrolyte layer, is mechanically pressed against the substrate. That way, the layer is transferred onto the surface by means of soft lithography techniques. The second step includes immersion of as-prepared surfaces in solvent with dispersed nanoparticles. These capped nanoparticles, of the polarity opposed to the polyelectrolyte layer, are electrostatically attracted to the surface, following only the patterns transferred in the first step. Self-assembly of the charged nanoparticles or microspheres[39] on the polyelectrolyte substrate is a well-known method for the preparation of monolayer nanoparticle surfaces.[40] Forces keeping the system together can also further guide 3D micro- and nanostructured assemblies.[28] These tandem polyelectrolyte−nanoparticle scaffolds act as preferable crystallization centers during metallization via the Tollens reaction (step three).[41] Metallizing of structures, hollow pores, has already been reported in the literature.[42] What is novel for the current research is the fact that the presented method creates any-shape 2D patterns uniformly covered with silver.

We demonstrate the feasibility of our method by producing a pattern of conductive lines, which, incorporated into an exemplary circuit, supports current flow and the flashing of LED. We believe that this approach can be used for rapid prototyping of 2D electronics of all shapes with macroscale applications. It can be used for the assembly of micrometer-sized antennas, sensors, or simple connectors, which nowadays are often incorporated in wearable electronic systems, usually combined with triboelectric power generators.[43] Our goal was to find alternative methods for electric circuit patterning, somewhat limited in resolution, but fast, cheap, and requiring little or no laboratory-grade equipment. Furthermore, unlike classical circuit prototyping, our processing route needs no additional protective layers or chemical resists, except for the creation of replica molds.

MATERIALS AND METHODS

Materials. Positive photoresists form an AR-P 3700 series, produced by Allresist. $AgNO_3$ (99.9%), $NH_3{\cdot}H_2O$ (30%, pure for analysis), and NaOH (pure for analysis) were purchased from POCH (Avantor, Gliwice, Poland). Citric acid ($C_6H_8O_7$), glucose ($C_6H_{12}O_6$), trichloro(1,1,2,2-perfluorooctyl)silane (silanizing agent), and polyethylenimine (PEI; average Mw ∼750,000, 50% w/v in H_2O) were purchased from Sigma-Aldrich. Polydimethylsiloxane (PDMS) was purchased from Dow Corning under the name Sylgard 184 Silicone Elastomer Kit. All reagents were used without further purification. Polyelectrolyte solutions were prepared in HPLC-grade water from Sigma-Aldrich to prevent contamination and ionic effects. For the other steps, water from the Hydrolab HLP10UV water system was used.

Preparation of Replica Mold Masters. Samples were prepared in the cleanroom of class 100 (AGH UST, Academic Centre for Materials and Nanotechnology, Krakow, Poland), equipped with maskless MicroWriter ML3 Pro (385 nm light source). The radiation dose was 140 mJ/cm^2. The designed patterns were lines with the following dimensions: 10/15 and 25/50 μm (line width/distance between lines). For the prototype electrical device, the dimensions of the electrodes were 4 × 4 mm^2. In order to pattern design, open source KLayout software was used. Before the photoresist deposition process, the silicon substrates (1 × 1 or 2 × 2 cm^2, Siegert Wafer, boron-doped, <100>, resistivity 1−30 Ω·cm) were cleaned. First, they were washed with acetone and dried using N_2. Then, they were washed with distilled water and dried using Ar. Next, they were immersed in acetone and sonicated for 10 min at 50 °C. After that, they were dried using Ar. This step was then repeated with immersion in methanol. The cleaned silicon substrates were heated to 100 °C and placed into a spin coater. A small amount of photoresist was added on top (typically 100 μL for 1 × 1 cm^2 and 300 μL for 2 × 2 cm^2 silicon substrates) to cover the whole surface in a thin layer. The following parameters were used for the spin-coating process: 6000 rpm for 45 s. After the process, the substrates were placed on a hot plate for 1 min at 100 °C. After UV exposure, the mold substrates were immersed in the developer (specific for the given photoresist) for 10 s and then put into the H_2O for 30 s. The final step was to place the substrates on the hot plate (115 °C) for 1 min.

Preparation of PDMS Stamps. The prepared molds were placed into a static vacuum in a desiccator with 50 μL of silanizing agent for 30 min. The next step was to flood the molds using the mixture of PDMS resin and hardener (10:1 by weight). Molds with resin were placed in a desiccator under dynamic vacuum conditions for 1 h and then placed in the dryer for 12 h at 65 °C. The PDMS stamp was mechanically cut out afterward.

AgNPs Synthesis. Silver nanoparticles (AgNPs) with citric acid as a capping agent were synthesized according to the modified procedure of Bastús et al.[44] Several growth and purification steps were executed, generating ∼9 nm nanoparticles. For the detailed synthesis procedures, see Section 1 in the Supporting Information. A synthesis procedure for positively charged nanoparticles is also presented there.

Preparation of Patterned PEI Layers on Substrates. Before the deposition of the polyelectrolyte layer, the silicon, glass, or polystyrene substrate and PDMS stamp (Figure 1A) were washed with isopropanol and distilled water, sonicated for 10 min, and then dried in Ar flow. Additionally, the substrates were placed into an oxygen plasma cleaner for 10 min. The PDMS stamps were immersed in the 1 mg/mL PEI solution in HPLC-grade water for 15 min (Figure 1B). The substrates were washed for 15 s by immersion in HPLC-grade water and dried in N_2/Ar flow. The dried PDMS stamp was put on the target substrate for 15 min at RT (Figure 1C) and

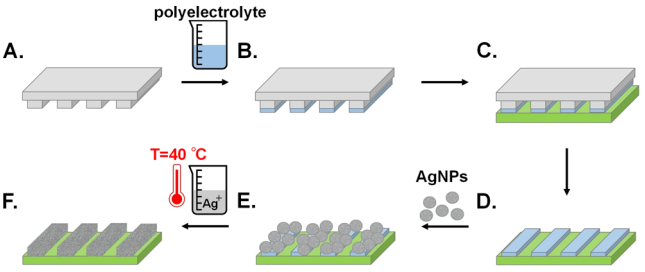

Figure 1. Fabrication of patterned conductive paths on an isolating silicon surface. (A) Preparation of the PDMS stamp with the desired microstructures by means of replica molding. (B) Polyelectrolyte adsorption on the PDMS stamp. (C) Transfer of a polyelectrolyte layer onto a target surface. Transfer effectiveness depends on the surface energy of the substrate. (D) Patterned polyelectrolyte paths on the surface. (E) Controlled addition of AgNPs (PEI-AgNPs), which act as preferred crystallization sites in (F) the Tollens reaction, resulting in the formation of conductive silver paths (PEI-AgNPs-Ag).

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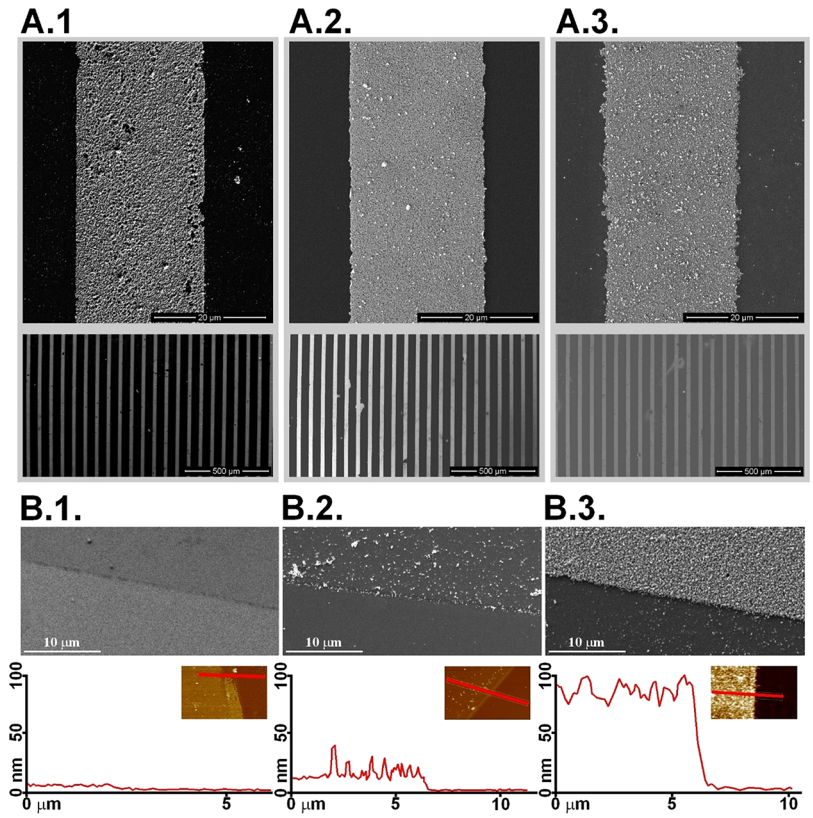

Figure 2. SEM images of PEI-AgNPs-Ag patterned paths (A. Top overview) on silicon (1), glass (2), and polystyrene (3) and (B. Borderlines) SEM images on the silicon surface with the corresponding AFM cross sections of patterned paths: (1) after adhesive transfer of PEI, (2) after adsorption of AgNPs (PEI-AgNPs), and (3) after crystallization of Ag (PEI-AgNPs-Ag).

then mechanically peeled off (Figure 1D). For the substrates with high surface energy,[45] good wettability, and low contact angle, the transfer of polyelectrolyte is easier to implement.[46] If not, extended oxygen plasma treatment on the cleaned substrate is recommended.

Fabrication of PEI-AgNPs Paths. The AgNPs solution was sonicated for 10 min before use. This step can be either omitted or the time can vary, depending on the particular situation—e.g., if the nanoparticles do not agglomerate upon storage. After the PDMS-PEI stamp patterns were transferred to the silicon, glass, or polystyrene surface, the samples were immersed for 30 min in the AgNPs solution. Then, the samples were washed thoroughly for 30 s by immersion in HPLC-grade water and dried in Ar flow (Figure 1E). This step determines if there are any unwanted crystallization centers left between pattern lines.

Fabrication of PEI-AgNPs-Ag Conductive Paths. Silver was deposited on the Si-PEI-AgNPs substrates using the chemical reduction process (the Tollens reaction).[42] $AgNO_3$ (0.13 g) was dissolved in 7.5 mL of water−ethanol (2:1, v/v) and heated to 60 °C. Next, 200 μL of 0.1 M NaOH solution was added. Then, a minimum of 300 μL of $NH_3{\cdot}H_2O$ was added to dissolve all precipitation, leaving a clear solution. The patterned silicon, glass, or polystyrene substrates with AgNPs were placed in the solution. Glucose (80 mg) was dissolved in 2 mL of the water−ethanol (2:1, v/v) solution and added to the previously prepared mixture of $AgNO_3$, NaOH, and NH_3. The deposition of the silver took usually 4 min (for 90% of the prepared samples). The growth rate of Ag was dependent on the number of crystallization centers and the temperature of the Tollens reaction. An increase in both of them shrunk the time window for good-quality metallic patterns to seconds (for a temperature of 90 °C). In the manuscript, the optimal conditions are provided, for a sample-to-sample repeatability and the process to occur within minutes. More information can be found in the Supporting Information (Section 8). After the reaction, the substrate needs to be once again thoroughly washed for 10 s by immersion in distilled water and dried in Ar flow (Figure 1F).

Characterization. Nanoparticle size and charge were measured with Zetasizer Nano ZS (Malvern Panalytical) in the configuration for a measurement angle of 173°. The structures and morphologies of the prepared samples were examined with a scanning electron microscope (SEM; FEI Quanta 3D 200i) at accelerating voltages of 2 and 5 kV and with an optical microscope in the light field mode (Nikon Eclipse LV150N). Moreover, topography, thickness, and conductive parameters were examined using atomic force microscopy (AFM). Images were obtained with a Dimension Icon XR (Bruker, Santa Barbara, CA) working in the PeakForce Tapping (PFT) mode in the air using standard silicon cantilevers with a nominal spring constant of 0.4 N/m. PeakForce TUNA mode was used for conductivity imaging with a bias voltage equal to 100 mV and for collecting $I-U$ curves from the random spots on the PEI, PEI-AgNPs, PEI-AgNPs-Ag surfaces, and reference silicon. Conductive Pt/Ir probes with a nominal spring constant of 0.4 N/m and a nominal curvature radius of 25 nm were used for all electrical measurements. The data for $I-U$ plots for all samples were gathered under the same conditions, using the ramp mode with a setpoint value corresponding to a maximum force of 1 nN. The voltage applied between the tip and the sample surface was ramped in the range of −200 to 200 mV. The plots were recorded in at least 50 random points for each sample, and conductivity was given in S/m. Finally, four-point probe measurements were done on Keithley 4200 SCS with currents of 1−100 μA to outer electrodes. The voltage was measured between inner electrodes, and the final sheet resistance was given in Ω/sq.

Theoretical Model Simulations. The electric field gradients and NPs deposition process were solved numerically using COMSOL Multiphysics 5.4.[47] The model was based on ACDC, Chemical Engineering, and Particle Tracing modules. All simulations were performed in a two-dimensional geometry. A detailed description of

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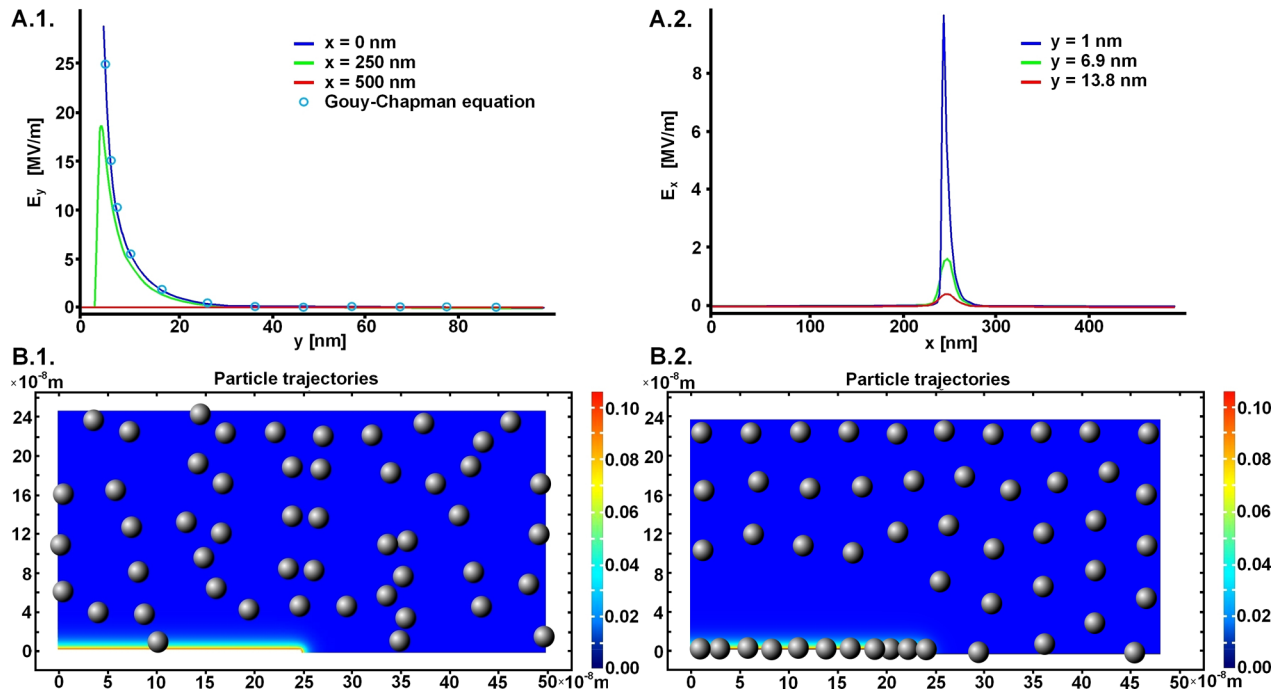

Figure 3. (A) Components of the electric field: (1) vertical (E_y) and (2) horizontal (E_x). E_y was plotted at three positions at x = 0 nm, x = 250 nm, and x = 500 nm. E_x was plotted at three positions above the line/electrolyte interface at y = 1 nm, y = 6.9 nm, and y = 13.8 nm. (B) Snapshots of the AgNPs adsorption process on a charged PEI pattern, shown at t_{start} (B.1) and t_{end} (B.2).

the parameters used is presented in Section 4 in the Supporting Information.

RESULTS AND DISCUSSION

Fabrication and Characterization of Conductive Paths. To construct the conductive paths on the flat silicon surface, we first transferred a thin polyelectrolyte layer from a PDMS replica mold with the pattern of parallel lines onto a cleaned surface of silicon, glass, or polystyrene. In the next step, the substrate with the polyelectrolyte pattern was immersed for 30 min in a solution of recently synthesized AgNPs (for details, see Section 1 in the Supporting Information) capped with negatively charged citric acid molecules. The size dispersion of nanoparticles does not play a crucial role at this stage—nanoparticle pattern acted as a scaffold in the next step of the process. The resulting hybrid polyelectrolyte−nanoparticle pattern (PEI-AgNPs) was washed and immersed in the Tollens reagent. The resulting substrate with PEI-AgNPs-Ag conductive paths was then used in further experiments.

The silicon substrates obtained in each step of the procedure were examined using SEM and AFM. As shown in Figure 2B.1, the conductive pattern assembly starts by transferring the PEI monolayer, developed with layer-by-layer (LbL) methodology, resulting in uniform transfer of the nanofilm onto a silicon substrate. The typical PEI coverage in the middle of the macroscopic pattern was measured to be 3.6 ± 0.3 nm, with an RMS roughness of 0.2 ± 0.1 nm, a value higher than the typical polyelectrolyte monolayer prepared by immersive assembly (thickness of 1−2 nm).[48,49] This difference in the PEI layer thickness can be caused by the fact that the layer is being transferred by stamping, instead of being directly grown from solution—similar to roll-to-roll processed films.[50] As a reference, the bare PEI monolayer on a silicon wafer, obtained from a solution, reached a thickness of 1.9 ± 0.1 nm (see Figure S6 in the Supporting Information). This typical thickness value of the bare PEI monolayer confirms that the increased thickness of the patterned PEI layer is related to the process of transferring it from the PDMS stamp. Immersion and AgNPs deposition caused changes in both the average surface height and surface roughness—for the sample denoted as PEI-AgNPs. Easily recognizable nanoparticle clusters (Figure 2B.2) had increased the thickness of the layer to up to 26.2 ± 2.5 nm and the RMS to 4.1 ± 0.8 nm. This was in line with the DLS size distribution of AgNPs. Moreover, AgNPs cover the polyelectrolyte film in a homogeneous way—as expected from the electrostatically driven interaction (attraction) of nanoparticles with the polyelectrolyte layer. In contrast, the bare silicon substrate cannot hold nanoparticles at the surfaces while being washed with water due to the lack of the necessary electrostatic interactions. This behavior allows efficient conductive surfaces to be fabricated only in the desired areas, yet due to electrostatic interactions, particles do not construct a continuous layer. Taking the above into consideration, the Tollens reaction was carried out to improve the continuity and conducting properties of the thin patterns obtained. The AgNPs electrostatically attracted to the PEI layer behaved as crystallization seeds for uniform and continuous silver layer formation. A fully functionalized PEI-AgNPs-Ag pattern is shown in Figure 2A.1 and 2B.3. The thickness of the layer had increased to 81.4 ± 8.6 nm, with an RMS roughness of 18.3 ± 1.8 nm. Allowing the Tollens reaction to run for elongated periods of time or in higher temperatures or with more concentrated substrates resulted in either coverage of both treated and untreated surfaces or production of a thicker (>100 nm) yet more rough top surface of patterns. For these reasons, the metallization processing procedure needed prior optimization steps—regarding reaction time, temperature, and substrate concentrations. The

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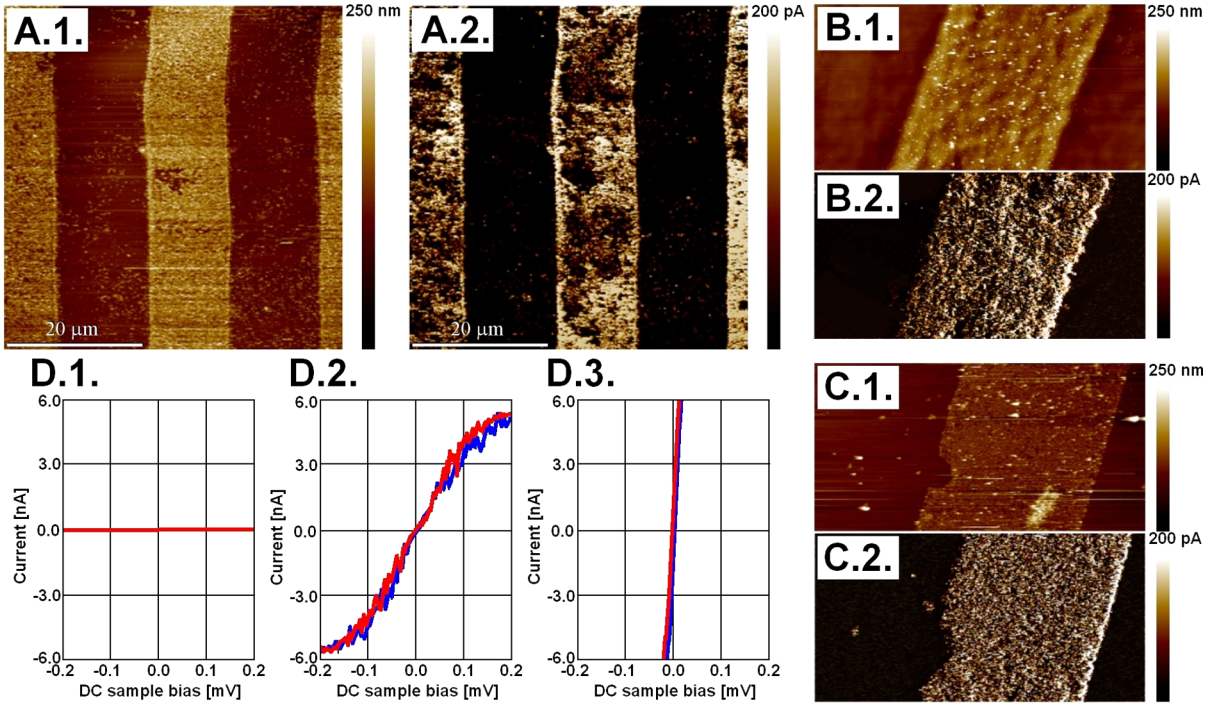

Figure 4. (A) AFM PF-TUNA images of PEI-AgNPs-Ag: (1) topography and (2) current on silicon (A), polystyrene (B), and glass (C) substrates. All images are in the same scale, presented beside the figures in A. (D) Representative $I-U$ plots of layers on silicon: (1) PEI, (2) PEI-AgNPs, and (3) PEI-AgNPs-Ag.

process was deemed completed after either microscopic evaluation of pattern quality or conductivity measurements.

The described procedure is universal for different substrates—conducive paths were obtained also for glass (Figure 2A.2) and polystyrene (Figure 2A.3) substrates and were very close in construction to their analogue on silicon. The quality and homogeneity of patterned structures ensure the continuity of both layers on a small and a macroscale. For paths on the polystyrene substrate, the edges are not as clear as in the case of other substrates, which is due to the significant roughness of the substrate.

Metallic patterns can be created as positive or negative regarding patterns on the initial PDMS stamp. This effect can be controlled by a proper choice of polarities of both polyelectrolytes and nanoparticles. Section 2 in the Supporting Information contains exemplary results of the silicon substrates covered uniformly by poly(sodium-4-styrenesulfonate) (PSS)—a polyelectrolyte of negative polarity. On top of the positively polarized PEI pattern was stamped. Finally, the sample was immersed in positively charged AgNPs. That way, inverted scaffolds were created, as only the negatively polarized surface, not protected by the PEI layer, was covered with AgNPs. The metallic pattern was inverted with respect to the pattern obtained following the procedure described in the main text.

A nanoparticle-based scaffold is a necessity for the final metallic pattern to appear. Otherwise, when omitting the nanoparticle assembly step, concomitant metal crystallization will take place on the whole surface of the substrate. This happens even despite the fact that the silicon substrate is PEI-patterned (Section 3 in the Supporting Information).

Theoretical Prediction of the Electrostatically Driven Nanoparticle Agglomeration Process. We modeled the electric field over an area where positively charged and non-charged lines meet. Based on the experimental data, we estimated the thickness of the deposited polymer to be 5 nm; hence, the lines have an interface with the surrounding electrolyte solution at y = 5 nm and y = 0 nm for the charged and non-charged parts, respectively. The details on the geometry of the system are given in Section 4 and shown in Figure S4 in the Supporting Information. The results of electric field screening are shown in Figure 3A,B. A nonzero value of field components indicates that there is an electrostatic force acting on the nanoparticles. Its primary role is associated with the E_y component, as it attracts particles vertically to the charged surface and stabilizes the deposit. At the point of contact of both lines, there is also a nonzero horizontal force component that leads to the migration of particles from the area over the non-charged line toward the charged interface. Despite the fast decay of the electric field, with a Debye length of λ_d=6.9 nm, the electrostatic force is effective at attracting nanoparticles from a distance of up to ∼100 nm into the solution. This is visible in Figure 3B.2 as the depletion zone surrounding the charged line interface. The deposition process, from the random distribution of NPs at t_{start} to the final state at t_{end}, is shown in Figure 3B. To trace the adsorption kinetics of this process, we introduced the dimensionless surface coverage factor θ, defined as $\theta = N_d/N_{dmax}$, where N_d is the number of deposited NPs and N_{dmax} is the maximum number of particles that can be arranged into a 1D monolayer on the surface of the charged line. For the purpose of this simulation, N_{dmax} = 14.53. To validate the model, we compared our results for field screening with the analytical form of the Gouy−Chapman theory suitable for planar interfaces.[51] As shown in Figure 3A, we obtained perfect agreement between both solutions. More on the adsorption kinetics and theoretical calculations can be found in Section 4 in the Supporting Information.

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Conductivity Determination. Non-functionalized surfaces of the bare silicon maintained their insulating properties (average sheet resistance on the order of 9×10^3 Ω/sq), whereas fully functionalized PEI-AgNPs-Ag surfaces achieved macroscopically measured sheet resistance on the order of 9×10^1 Ω/sq. Sheet resistance was measured for samples without patterns—i.e., fully covered by layers of substrates—PEI, AgNPs, and Ag polycrystalline film form the Tollens reaction. Moreover, the PEI-AgNPs-Ag paths were found to be highly conductive, as shown in the AFM images captured in the PF-TUNA mode (Figure 4A.1) and in the AFM current−voltage ($I-U$) plots captured in the spectroscopic mode (Figure 4A.2). The current map of the PEI-AgNPs-Ag paths exhibits high conductance for all modified surfaces. This is consistent with the homogeneous coverage of the PEI path with the AgNPs and metallic silver after the Tollens reaction (Figure 4 and Figure S7 in the Supporting Information). Similar results were obtained for PEI-AgNPs-Ag patterns on polystyrene (Figure 4B) and glass (Figure 4C). The conductivity measurements at the nanoscale in the system studied rely on the electrical contact between the AFM probe and the conductive surface of the paths.[52] This contact may vary slightly from one $I-U$ curve to another, as the roughness of the surface determines the contact area between the AFM probe and the surface. However, the narrow distribution of the measured conductance (dI/dU) allows calculations of the electrical conductivity (σ) for the fabricated samples. Based on the plots shown in Figure 4D.3 and calculations described in Section 7 in the Supporting Information, the electrical conductivity of PEI-AgNPs-Ag can be estimated to be 1×10^4 S/m, which is two orders of magnitude higher than that measured for the PEI-AgNPs sample before the Tollens reaction (2×10^2 S/m, plot presented in Figure 4D.2). The current−voltage characteristic of PEI-AgNPs-Ag paths resembles the one for linear resistor, whereas PEI-AgNPs paths are conductive only in small potential ranges—from −100 to +100 mV. For higher potentials, nonlinear response is registered, limiting eventually the current, a behavior describing devices with high internal resistance. The value of σ for PEI paths on the silicon surface (Figure 4D.1) was estimated to be 7×10^{-4} S/m, which is slightly higher than the value for the bare silicon (3×10^{-4} S/m) measured in the reference and the value for the non-covered areas between PEI-AgNPs-Ag paths. It is worth mentioning that to keep the process suitable for electric circuit prototyping, the conductivity contrast between different types of surfaces (treated vs untreated) should exceed 10^3 S/m,[53,54] which can easily be achieved with the fabrication method proposed here.

Macroscale Working Electrical Circuit. The conductive PEI-AgNPs-Ag paths on silicon wafers were used as a passive element in an exemplary electrical circuit presented in Figure 5. The paths fabricated on a silicon wafer patterned with an array of 277 parallel lines (20 mm long, 25 μm wide, separated by 50 μm) were arranged on a 20×20 mm^2 square. In the middle of each edge of the square was a metallic pad. Parallel lines ran through all the available space, creating a 20 mm long conductive path between opposite pads. The idea behind the design was to show the 2D anisotropy of the surface conductivity, so two opposite pads were connected with a PEI-AgNPs-Ag path, while two others were not. As shown in Figure 5A, for the circuit wires connected to nonbonded pads, the red LED did not flash, indicating no current flow. As expected, in this configuration, the circuit was not closed, resulting in the lack of electric conduction. In contrast, when the wires connected to the opposite pads were bonded together with patterned PEI-AgNPs-Ag paths (Figure 5B), this caused the diode to light up. That is clear evidence that the patterned and then metalized surface is capable of sustaining current flow. Furthermore, the fabrication of a working circuit confirms that the presented method is not only feasible but can be implemented in the production of macroscale devices. Another example of a macroscale pattern substrate on a 45×25 mm^2 surface was fabricated without any inconvenience (see Figure S11 in the Supporting Information).

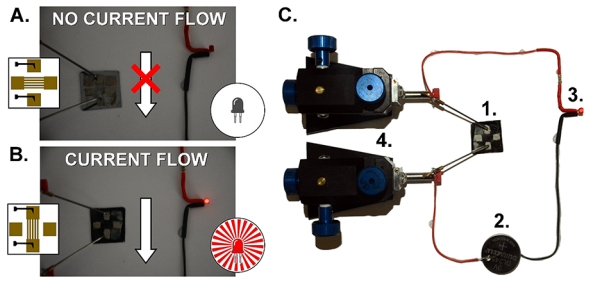

Figure 5. The prototype electric circuit built from an isolating silicon wafer patterned with 10 mm long AgNPs-based conductive paths. (A) No current flows through the paths oriented perpendicularly to the power source. (B) Parallel orientation of the paths with respect to the power source allows for current flow. (C) A photo of the prototype: (1) a silicon wafer with conductive paths, (2) a 3 V battery, (3) a red LED attached to a 100 Ω resistor, and (4) micromanipulators.

CONCLUSIONS

This work demonstrates a practical use of a facile, fast, and cheap method of enhanced assembly of silver conductive nanoparticles into patterns, guided by polyelectrolyte (polyethylenimine (PEI)) 2D scaffolds stamped on different rigid surfaces—silicon, glass, or polystyrene. The agglomeration of colloidal AgNPs results in semi-conductive paths (10^2 S/m). The only requirement for the agglomeration to happen is for the surface charge of nanoparticles to be of opposed polarity to patterned polyelectrolyte lines. The conductive properties of nanoparticle decorated patterns can be easily enhanced by the Tollens reaction, resulting in further crystallization of Ag on already present centers (AgNPs). The whole process takes place in 60 °C and yields patterns of increased conductivity (10^4 S/m). Structures are produced with micrometer resolution. They are characterized by high uniformity (<100 nm thickness, <20 nm roughness) and span across macroscopic scale areas (~2 cm).

Through the course of the current publication, we demonstrated that the effects of electrostatic attraction can be made pattern-selective. By means of simple procedures, thin-layer transfer stamping and rigid substrate immersion in different solutions, it is possible to functionalize the areas of several cm^2. An increase in the electrical conductivity is first ascertained by nanoparticles covered with a polar capping agent and additionally by further agglomeration of a metal. The most crucial step in the process is the initial concentration of the functionalized nanoparticles where the pattern is to form. This limits further functionality, as for some applications, the distance between particles must be specified. For example, to support minimal electric current flow, the particles should be interconnected. The latter could be done by increase of nanoparticle concentration or by vortex-assisted assembly.[55]

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Many ideas of preparing 2D shapes made out of nanostructured silver have been scattered throughout the literature, yet no ultimate all-substrate, low-temperature, high-yield, large-area process has been found so far. What is unique with the method presented is the fact that laboratory-grade equipment is needed only during the production of customized master for PDMS stamps. Later, only three simple technical steps are needed for device scaffold assembly—stamping, immersion, followed by further chemical metallization. Each of these procedures consumes relatively cheap and abundant ingredients only. Such an approach is surprisingly not so common, and usually functional patterning requires more involvement from the researchers—either several laser scans,[56] an increased number of different techniques of sample fabrication,[57] or the need for repeated processing.[58] In some cases, only one specific substrate is compatible,[59] as the origin of pattering is based on chemisorption. In other cases, one can directly transfer nanostructures on a variety of substrates,[60] yet must use a shadow mask for every transfer. Some of the methods use polymeric stamps to carve out desired patterns from the pre-functionalized substrates—e.g., with nanowires dispersed on the surface.[61] Compared to the previous methods, the one presented here can deliver patterns of better resolution and with lower conductive surface roughness. To stay objective though, the ideas mentioned before result in either similar or even better sample surface conductivity. Some of the superior quality techniques unfortunately lack patterning options[62] or produce samples with higher roughness.[63]

As far as future advancement is deliberated, the most obvious addition to sample processing would be to include temperature annealing, leading to the improvement of the electrical conductivity of samples. Other improvements would include the use of polar nanoparticles with fluorescent properties, including fluorescent probe-modified metallic nanoparticles or perovskite nanostructures. Polar magnetic nanoparticles can also be used as functional moieties to generate microscale any-shape magnetic fields. The presented technique should also be optimal for another type of nanostructures, such as nanowires or nanoflakes. For substrates with surface energies high enough, the first part of the process, transferring of the polyelectrolyte pattern, could be implemented on non-flat or flexible substrates. To achieve better quality of patterns, the polyelectrolyte patterning technique should be automated in future implementations.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsanm.2c02559.

Synthetic procedures and characterization of AgNP, details on the electric field modeling and deposition of AgNPs, and estimation of the conductivity of PEI-AgNPs and PEI-AgNPs-Ag paths (PDF)

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Notes

The authors declare no competing financial interest.

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