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Picosecond Time-Scale Resistive Switching Monitored in Real-Time

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The resistance state of filamentary memristors can be tuned by relocating only a few atoms at interatomic distances in the active region of a conducting filament. Thereby the technology holds promise not only in its ultimate downscaling potential and energy efficiency but also in unprecedented speed. Yet, the breakthrough in high-frequency applications still requires the clarification of the dominant mechanisms and inherent limitations of ultra-fast resistive switching. Here bipolar, multilevel resistive switchings are investigated in tantalum pentoxide based memristors with picosecond time resolution. Cyclic resistive switching operation due to 20 ps long voltage pulses of alternating polarity are experimentally demonstrated. The analysis of the real-time response of the memristor reveals that the set switching can take place at the picosecond time-scale where it is only compromised by the bandwidth limitations of the experimental setup. In contrast, the completion of the reset transitions significantly exceeds the duration of the ultra-short voltage bias, demonstrating the dominant role of thermal diffusion and underlining the importance of dedicated thermal engineering for future high-frequency memristor circuit applications.

1. Introduction

Due to the self-assembling, atomic-scale formation, or destruction of their conducting channels, filamentary memristors[1–8] simultaneously exhibit the key properties seeked for the hardware elements of future computational architectures.[9–13] Ultimate downscalability is granted by the single atom level control of the filament formation.[14,15] In addition to sub-nanometer filament diameters, devices with 2×2 nm^2 electrode cross-section areas were also demonstrated.[16] The analog tunability of the filaments were exploited in large crossbar arrays performing vector-matrix multiplications in only one computational step at greatly reduced power consumption.[17–20] Furthermore, the bias voltage dependent, highly nonlinear dynamical properties of the resistive switching[21,22] were employed to realize reservoir computing architectures based on only a few physical nodes[23] as well as to prevent undesired leakage currents in memristor crossbar arrays.[24]

It is also conceivable, that the relocation of only a few atoms upon resistive switching must be feasible at an extremely fast pace, qualifying memristors to enter the frequency domain of cutting edge telecommunication technologies. Oxide and nitride based devices have indeed been tested to fast resistive switching induced by individual voltage pulses[25–31] as short as 50 ps,[32,33] while circuit design considerations[31,34,35] and molecular dynamical simulations[36] predict a possibility for up to two orders of magnitude faster operation, bringing even Terahertz frequency applications in sight. Yet, to date memristors have merely been implemented as static switches in broadband circuits,[37] where their potential of ultra-fast switching operation was not exploited. In order to optimize memristor devices for high-speed operation in real circuits, the identification of the dominant switching mechanisms as well as the microscopic and design-related speed limitations is inevitable. Beyond verifying the equilibrium resistance states between ultra-fast programming voltage pulses, this requires the real-time analysis of the switching dynamics also during the pulses.

Here we present alternating resistive switching and multilevel programming in tantalum-pentoxide based memristors due to 20 ps full width at half maximum (FWHM) set and reset

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pulses, confirmed by the evaluation of the steady states before and after the programming pulses. More importantly, we move beyond the common approach of verifying the effect of the programming pulses in the established steady state only: We have developed an optimized sample design which enabled us to monitor the dynamics of the resistive switching also during the ultra-short programming voltage pulses, thereby set times well below 20 ps pulse durations could be measured at picosecond resolution. In addition, a thermal delay of the reset transition, which exceeds the reset voltage pulse duration, was discovered. The latter also allows the experimental separation of electric field induced and diffusion driven resistive switching mechanisms. The intrinsic, structural, and instrumental speed limitations of resistive switching are evaluated both in the set and reset direction, facilitating low-power memristor circuits for telecommunication technologies as well as ultra-fast neuromorphic computing applications.

2. Results and Discussion

Our report is structured as follows. First, the memristor structure and the principles of the transmission measurements of fast voltage pulses are summarized. Next, following the more traditional approach, alternating resistive switchings due to ultra-fast voltage pulses down to 20 ps FWHM are evaluated in the steady high resistance (HRS) and low resistance (LRS) states, exhibiting multilevel programming and satisfying the "voltage-time dilemma."[21,22] Moving an important step further, we assess the criteria of experimentally resolving resistive switchings *during* the ultra-fast voltage pulses and, accordingly, demonstrate set switching times at the picosecond time-scale. Finally, also by analyzing the time dependence of the transmitted voltage during the reset pulses, we provide experimental evidence that the thermally driven reset transition can take place at longer time-scales than the actual reset voltage pulse width.

2.1. Memristor Structure and DC Characterization

The device structure and the individual thicknesses of the vertically stacked layers are shown in **Figure 1**a. The Pt bottom electrode was evaporated onto a standard Si/SiO_2 wafer using a thin Ti adhesive layer. The 5 nm thick Ta_2O_5 switching layer, the Ta top electrode, and the Pt cap layer were deposited by high-power impulse magnetron sputtering. The lateral patterning of the devices was carried out by standard electron beam lithography and lift-off. Figure 1e illustrates the coplanar waveguide structure hosting the device under test. For this purpose 200 nm thick Au electrodes were evaporated using a resist mask defined by standard optical lithography. The subsequentially magnified electron microscope images in Figure 1f,g provide an insight into the electrode layout and the 180 nm × 150 nm overlaying area of the top and bottom electrodes. Further fabrication details and considerations on the sample layout are detailed in Experimental Section.

The dc performance of the $Ta/Ta_2O_5/Pt$ devices are summarized in Figure 1b–d, exemplifying the typical, hysteretic current–voltage ($I(V)$) traces, their cycle-to-cycle reproducibility and routinely obtained endurance over 1000 consecutive operation cycles. The statistical analysis of the zero bias resistance values in Figure 1d reveals a narrow distribution of the LRS around $R_{LRS} \approx 2$ kΩ and a broader set of the HRS with R_{HRS} in the 10 – 30 kΩ range. The latter corresponds to the regime of the quantum conductance $G_0 = 2e^2/h \approx 77.5$ μS which is commonly regarded as an indication that the conducting filament is connected by only a few atoms in its narrowest cross-section. However, unlike in noble metals, the conductance histograms of nanowires made of transition metals do not exhibit any dominant features around integer multiples of G_0.[38] Therefore, the identification of few-atomic filament configurations in this conductance regime requires a more dedicated experimental analysis.[15,39] The larger spread of the R_{HRS} values compared to the one of R_{LRS} is commonly observed in Ta_2O_5 memristors.[2,3,32] It is attributed to the larger sensitivity of the conductance to the actual position and coordination of the atoms at the narrowest, few-atom wide filament cross-section, where a perfect structural reproducibility is not expected under the strongly out-of-equilibrium conditions prevailing during repeated resistive switchings. In conclusion, in the resistance regime shown in Figure 1d the conducting filaments are only partially destructed in the HRS while the LRS traces show good linearity up to the switching threshold. This is not only favorable for analog multilevel operations[19] but also ideal for the optimum resolution in the transmission experiments of high-speed voltage pulses outlined in the following.

2.2. Resistive Switching Due to Ultra-Short Voltage Pulses

The schematics of the fast pulsing setup is shown in Figure 1i. A programmable 100 GSa/s DAC board system was utilized as an arbitrary waveform generator (AWG) capable of firing voltage pulses down to 20 ps FWHM at 20 ps rise time. The voltage output of the AWG was further amplified up to ±4 V peak values by a broadband amplifier module specified to a 65 GHz analog bandwidth. The voltage signals propagated in 30 cm long, 65 GHz bandwidth, 50 Ω terminated coaxial RF cables. The memristor sample was engaged by two 67 GHz bandwidth triple probes in a custom-built probe station. The V_{TRANS} transmitted voltage signals were recorded by a 50 Ω terminated digital storage oscilloscope (DSO) operated at a 256 GSa/s sampling rate and 113 GHz analog bandwidth. A further enhanced, picosecond time resolution was achieved by taking advantage of the high reproducibility of the repeated switching cycles, as discussed later in Section 2.4. The V_{IN} signal was recorded separately by bypassing the memristor sample, the probes and the last cable section.

The equivalent circuit model of the memristor device is drawn in Figure 1h. This is composed of a series resistor R_S, a parallel capacitor C_{MEM}, and a resistor R_{MEM} representing the contributions of the lead and probe contact resistances, the parallel capacitance arising from the metal–insulator–metal stack of the memristor device and the memristive resistance, respectively. A numerical analysis revealing the influence of these circuit parameters on the measured V_{TRANS} voltage signal served as a guide to the optimization of the sample layout, as

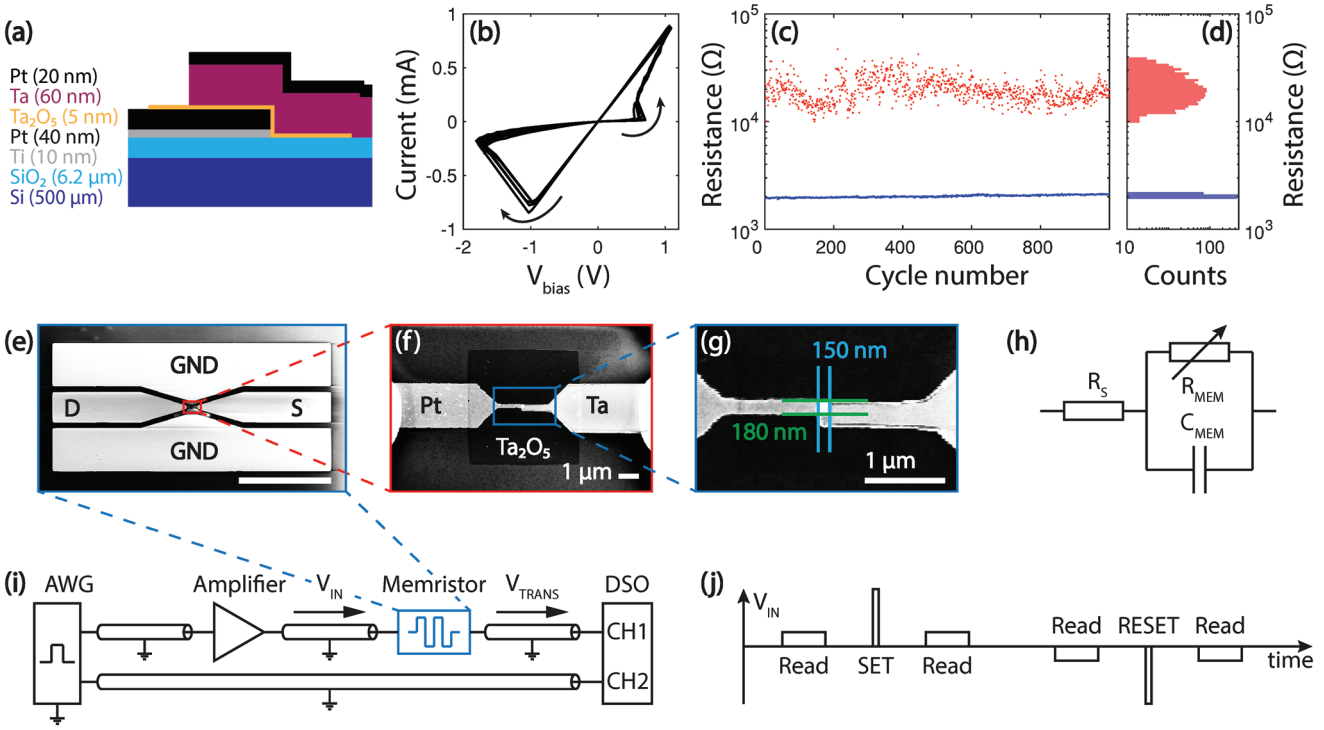

Figure 1. Device structure and the fast switching setup. a) The (not to scale) vertical cross-section of the memristor device. The layer sequence and the thicknesses are indicated on the left. b) Ten consecutive $I(V)$ traces acquired with an $f = 1$ Hz frequency and $V^0_{drive} = 2$ V amplitude triangular voltage signal. The arrows indicate the direction of the hysteresis. The dc setup is explained in the Experimental section. c) Illustration of the stability of the resistive switching operation over 1000 dc $I(V)$ cycles recorded at identical conditions to those in (b). The R_{LRS} (low resistance state, blue) and R_{HRS} (high resistance state, red) resistance values were evaluated from the zero bias slopes of the hysteretic $I(V)$ traces. d) Histograms of the R_{LRS} (blue) and R_{HRS} (red) data shown in (c). e) SEM image of the device embedded in a co-planar waveguide structure. The white scale bar in the lower right indicates 100 µm. The width of the planar gap is 4 µm. f) A magnified view of the memristor device with the Pt bottom electrode on the left and the Ta top electrode on the right. g) A further zoom into the device area shows the measured overlap area of 180 nm × 150 nm between the top and bottom electrodes. h) The equivalent circuit of the memristor device accounting for the lead resistance of the device as well as the contact resistance of the needle probes (R_S), the tunable device resistance (R_{MEM}) and the device capacitance arising from the vertical metal–insulator–metal stack (C_{MEM}). i) Schematics of the high-speed setup. The memristor device is exposed to the V_{IN} amplified voltage pulses provided by the arbitrary waveform generator (AWG). The V_{TRANS} transmitted voltage pulses are measured by a digital storage oscilloscope (DSO). The second output channel of the AWG is used to trigger the DSO. j) The (not to scale) schematics of the voltage pulse sequence repeated during the high-speed switching experiments.

discussed in Section 2.4 and in Experimental Section. In short, the real-time monitoring of the memristor's resistive response during the ultra-fast V_{IN} pulses critically relies on the careful minimization of C_{MEM} as well as further environmental parasitic capacitances but, at the same time, also requires the minimization of R_S.

Finally, the applied pulse scheme is illustrated in Figure 1j. In this work we demonstrate subsequent resistive switchings due to ultra-fast set and reset programming pulses without interrupting the measurement by dc cycling of the device. The low-bias readout of the equilibrium resistive state between the programming pulses was carried out by non-invasive, low-amplitude voltage pulses of 1 ns duration, preceding and following the 20 – 500 ps FWHM programming pulses by 10 ns. As a voltage polarity convention, positive bias corresponds to a higher potential applied on the Ta top electrode with respect to the Pt bottom electrode. The period of the set/reset cycle was 5.24 µs, the programming pulses of alternating sign followed at every 2.62 µs. In a "single shot" experiment 200 – 300 subsequent cycles were executed and recorded at maximum sampling rates.

The analysis of the device impedance based on the V_{TRANS} signal relies on the solution of the telegraph equations derived for our arrangement[40] which results in the formula of

$$\frac{V_{TRANS}}{V_{IN}} = \frac{2Z_0}{Z_{MEM} + 2Z_0} \quad (1)$$

where Z_{MEM} is the complex impedance of the memristor represented in Figure 1h and $Z_0 = 50\ \Omega$ is the wave impedance of the transmission lines. The time delay between the incoming and transmitted pulses arising from the propagation along finite cable lengths is compensated, as detailed in Section 2.4. We note that Equation (1) directly applies to plane waves and wave packages in the presence of a frequency independent, resistive Z_{MEM}. When a complex, frequency dependent $Z_{MEM}(f)$ is involved, the calculation of the time dependent V_{TRANS} response requires a Fourier analysis based on Equation (1) and $Z_{MEM}(f)$. Such numerical simulations are presented in Experimental Section.

As will be discussed later, the capacitive/resistive character of Z_{MEM} has a profound influence on the time-dependence of

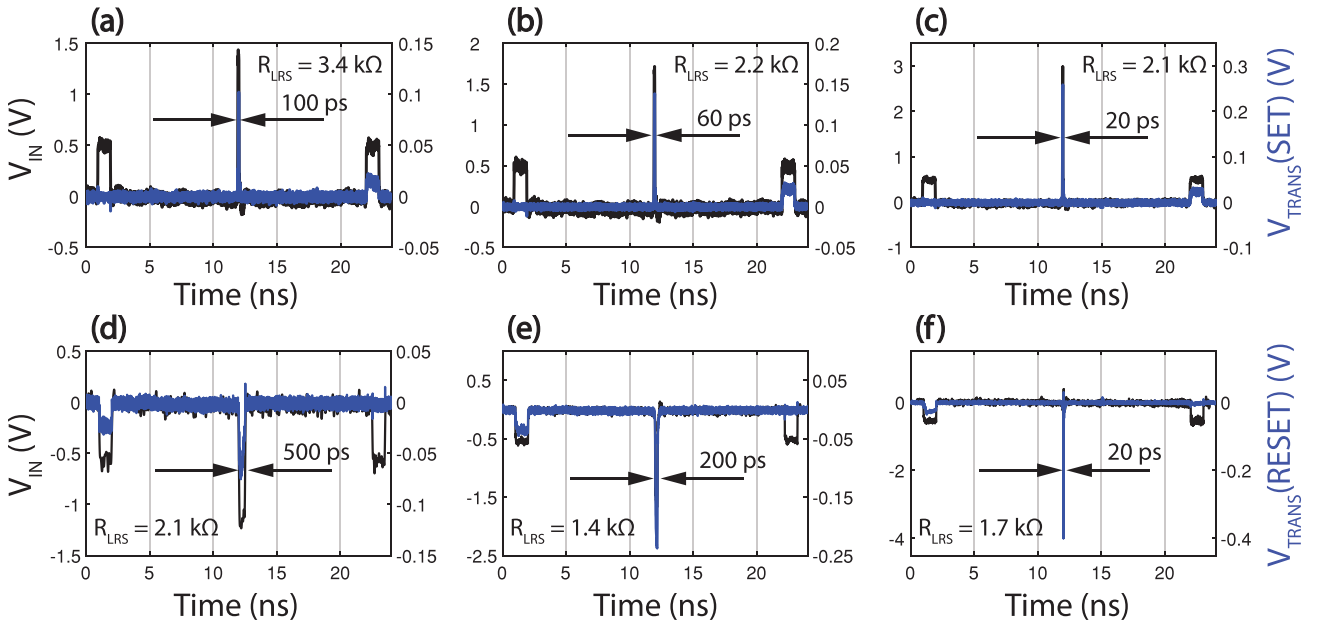

Figure 2. The effect of the fast set and reset pulses are monitored by 1 ns long read pulses in the steady state at various programming pulse durations, confirming resistive switching. a–c) Set operation due to 100, 60, and 20 ps voltage pulses, respectively. d–f) Reset operation due to 500, 200, and 20 ps voltage pulses, respectively. The left axes correspond to V_{IN} (black) whereas V_{TRANS}(SET) (upper panels, blue) and V_{TRANS}(RESET) (lower panels, blue) are scaled on the right axes. The R_{LRS} mean values evaluated by the 1 ns read pulses as well as the FWHM of the programming pulses are labeled on all panels. R_{HRS} > 20 kΩ. The data acquired during the programming pulses at picosecond time resolution are shown on a magnified scale in Figure 5 and discussed in Section 2.5.

V_{TRANS} during the ultra-fast programming pulses. However, during the 1 ns long read pulses a finite capacitive contribution to V_{TRANS} only arises at the steep, 20 ps long pulse edges. Owing to the low, C_{MEM} = 3 fF capacitance of our devices, V_{TRANS} between the edges of the 1 ns read pulse is exclusively dominated by the effect of R_{MEM}. Thereby, according to Equation (1), the V_{TRANS}/V_{IN} ratio becomes a real-valued number and the steady state resistance can be directly determined as $R_{MEM} = 2Z_0(V_{IN}/V_{TRANS} - 1)$.

In the following, we utilize this approach to evaluate the steady state device resistances before and after the ultra-fast programming pulses. The resistance resolution of this method is limited by the noise floor of the DSO at the voltage range needed to cover the V_{TRANS} signal also during the high-amplitude programming pulses. Consequently, the applied transmission method is able to resolve resistances in the $R_{MEM} \lesssim$20 kΩ regime with increasing resolution toward lower R_{MEM} values.

The electroforming step preceding the fast pulsing operation did not require the application of any dedicated, current limited dc voltage sweep. Instead, the pristine devices were exposed to the V_{IN} pulsing sequences illustrated in Figure 1j where the amplitude of the set pulse was gradually increased between the single shot experiments until stable resistive switching was established. More details about the pulsed electroforming scheme are provided in Experimental Section. After successful electroforming, the amplitude of the set pulse could be reduced again while cyclic resistive switching operation was still maintained until the threshold amplitude corresponding to the actual set pulse width was reached. As a matter of experience, this more gentle, pulse-based electroforming approach resulted in higher endurance and larger R_{HRS}/R_{LRS} ratios.

Set switchings due to programming pulses with 100, 60, and 20 ps FWHM and varying amplitudes are demonstrated in **Figure 2**a–c, respectively. Beside the set pulses, the 24 ns time interval of the panels also exhibits the 1 ns FWHM, V_{IN} = 0.5 V read pulses. The latter two parameters were adjusted in a way that, in the absence of a programming pulse, the read pulses do not induce any detectable resistive switching over 100's of cycles. The time axis of V_{TRANS}(SET) (blue, right axes) is compensated for cable length differences with respect to V_{IN} (black, left axes). The flat response to the first read pulse falls below the noise floor of the measurement confirming the HRS with R_{HRS} >20 kΩ at each displayed case. In contrast, the finite V_{TRANS}(SET) during the second read pulse testifies to the LRS with around 2 – 4 kΩ resistance, as labeled in the panels. Moreover, the finite resistive response during the set pulse indicates that resistive switching took place already within the duration of the latter (not resolved here).

Successful reset switchings triggered by 500, 200, and 20 ps long programming pulses were tested in a similar fashion to the set operation utilizing the second half of the scheme in Figure 1j, as shown in Figure 2d–f, respectively. After verifying that in the absence of a reset pulse they do not induce any reset transitions, 1 ns long and 0.5 V amplitude voltage pulses of negative polarity were utilized for the read operation. The finite V_{TRANS}(RESET) (blue, right axes) values during the first read pulses (black, left axes) clearly demonstrate that the device is prepared in the LRS of $R_{LRS} \approx$ 2 kΩ, as labeled in the panels. During the shorter programming pulses a

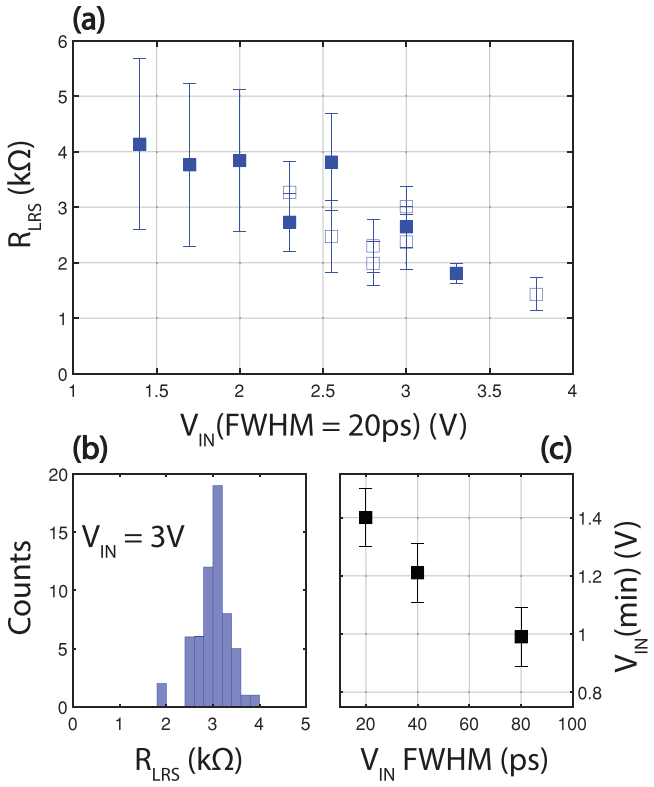

Figure 3. Multilevel programming in the LRS due to 20 ps FWHM set pulses and voltage–time dilemma in the sub-100 picosecond time domain. a) The tunability of the LRS by 20 ps FWHM set voltage pulses. The filled and empty squares represent R_{LRS} data acquired on two nominally identical devices. The symbols and the error bars correspond to the mean value and standard deviation of the resistance. They were determined by the 1 ns long, 0.5 V amplitude read pulses applied after each set pulse during a sequence of 50–100 alternating set/reset cycles, R_{HRS} > 20 kΩ. b) A representative R_{LRS} distribution corresponding to V_{IN} = 3 V. c) The pulse width dependence of the V_{IN}(min) lowest set voltage amplitude which induced resistive switching.

predominantly resistive response, characteristic to the LRS is observed (not resolved here), making the more involved time-dependent analysis outlined in the following sections necessary to determine the actual reset times. Nevertheless, the absence of a finite resistive response to the second read pulses unambiguously confirm the transition to the HRS with R_{HRS} > 20 kΩ.

2.3. Multilevel Programming

The effect of the 20 ps FWHM set pulse amplitude on the resistive switching is shown in **Figure 3**. First, R_{LRS} was statistically evaluated based on the resistive, real-valued V_{TRANS}/V_{IN} ratio harvested from the data acquired during the second read pulses over 50–100 consecutive switching cycles. Figure 3a shows the mean values (square symbols) and the standard deviations (error bars) of the calculated R_{LRS} distributions at each amplitude setting of the 20 ps FWHM set pulses. A representative R_{LRS} histogram corresponding to V_{IN} = 3 V is illustrated in Figure 3b. At the minimum V_{IN}(min) amplitude where resistive switching was observed at 20 ps FWHM, the LRS was found to exhibit $R_{LRS} \lesssim 5$ kΩ. The further monotonous, up to fivefold decrease in R_{LRS} with increasing V_{IN} shows the potential of multilevel programming using the shortest available set pulses. Figure 3c summarizes the V_{IN}(min) amplitudes as a function of the set voltage pulse duration in the sub-100 ps time domain. Here the error bars correspond to the discreteness of the amplitude adjustments arising from the six bit vertical resolution of the AWG. The observed linear increase of 0.2 V in the minimum amplitude at exponentially shortened pulse durations confirms that the general tendency expressed in the voltage–time dilemma sustains also in the so-far largely unexplored 20–100 ps regime. The obtained V_{IN}(min) values are in good quantitative agreement with the data reported by Witzleben et al.,[32] where the onset of the resistive switching was studied at fixed V_{IN} pulse amplitudes while the pulse width was swept in the 50 – 250 ps regime. We attribute the 10–30% lower pulse amplitudes found in our study to the differences in the actual oxide deposition and device layout parameters.

2.4. The Real-Time Monitoring Approach

In the previous sections resistive switchings due to ultra-short voltage pulses were demonstrated by investigating the equilibrium states before and after the pulses. However, this approach does not provide a real-time insight into the resistive transitions and, thus, only allows crude estimates of the involved time-scales. In order to take the next step, we analyze the time-dependence of the transmission during the V_{IN} pulses. We show that by an optimized device layout the equivalent circuit parameters introduced in Figure 1h can be adjusted such that a high contrast can be achieved between two reference traces, the non-switching HRS and LRS responses denoted in the following by V_{TRANS}(HRS) and V_{TRANS}(LRS), respectively. The resistive switching response will be quantitatively compared to these two references, all measured at identical V_{IN} bias. This comparison allows the deduction of the resistive switching time-scales.

For the ultra-fast V_{IN} pulses the transmitted signal is determined by the full Z_{MEM} complex impedance of the device according to Equation (1). A quantitative analysis about the tendencies on C_{MEM}, R_{MEM}, and R_S at 20 ps FWHM V_{IN} pulses is given in Experimental Section. In essence, at sufficiently low R_{MEM} and C_{MEM}, V_{TRANS}(LRS) is dominated by the resistive response of the device, resulting in a real-valued V_{TRANS}/V_{IN} ratio as illustrated by the black and green traces in **Figure 4**a. In contrast, at R_{MEM} >20 kΩ, V_{TRANS}(HRS) exhibits a merely capacitive character which is highly sensitive to C_{MEM} but much less to R_{MEM} and R_S, as shown by the red trace in Figure 4a. The duration of the resistive switching transition is identified as the crossover period of the V_{TRANS}(SET) or V_{TRANS}(RESET) switching response between the two reference traces, as demonstrated in Figure 4c.

Figure 4a illustrates 10 overlayed, highly reproducible consecutive cycles of the measured V_{TRANS}(HRS) (red, right axis) and V_{TRANS}(LRS) (green, right axis) responses due to 20 ps FWHM V_{IN} (black, left axis) set pulses. First, V_{TRANS}(HRS) was recorded in the pristine state, at a set pulse amplitude below the critical amplitude where electroforming occurs but above

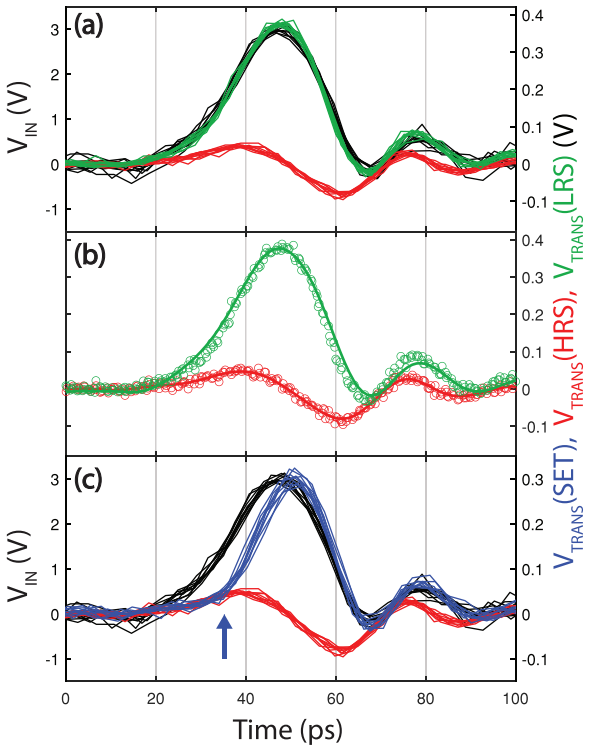

Figure 4. Analysis of the set switching during the programming pulse. In the non-switching LRS, the V_{TRANS}(LRS) response (green, right axes) is proportional to V_{IN} (black, left axes). In the non-switching HRS, the V_{TRANS}(HRS) response (red, right axes) is not proportional to V_{IN} due to the dominant capacitive contribution, but it is sufficiently suppressed due to the careful minimization of C_{MEM}. The V_{TRANS}(SET) set switching response (blue, right axis) exhibits a crossover between the above two reference traces which allows the identification of the switching time. a) The overlaying of ten consecutive, 20 ps FWHM V_{IN} set voltage pulses (black, left axis) as well as the corresponding, non-switching V_{TRANS}(HRS) (red, right axis) and non-switching V_{TRANS}(LRS) (green, right axis) responses demonstrates the cycle-to-cycle reproducibility and the resulting enhanced time resolution. b) The empty symbols correspond to the same data as in (a). The solid lines show the simulated transmissions calculated from the measured V_{IN} signal using the fixed $R_S = 350\ \Omega$, $C_{MEM} = 3$ fF, and R_{MEM} corresponding to HRS (red) and LRS (green), in accordance with the equivalent circuit shown in Figure 1h. More details about the transmission simulations are provided in Experimental Section. c) V_{IN} (black, left axis) and V_{TRANS}(HRS) (red, right axis) as in (a). The V_{TRANS}(SET) traces (blue, right axis) show ten consecutive, overlayed set switching response pulses of the same device, demonstrating the real-time resolved crossover between the corresponding initial HRS and final LRS. The blue arrow marks the starting of the set transition.

the minimum threshold of resistive switching in the electroformed state. Although the ≫MΩ pristine state is not to be confused with the >20 kΩ HRS, due to the dominating effect of C_{MEM} at higher R_{MEM} values, they result in experimentally identical V_{TRANS} responses. Thus, the transmission recorded in the pristine state provides a proper, non-switching HRS reference for our time domain analysis. After successful electroforming at a higher voltage level, the switching response was acquired at the reduced set pulse amplitude corresponding to the previously recorded HRS response. Finally, the non-switching LRS response was recorded at an identical set pulse amplitude by reducing the reset pulse amplitude, shown in Figure 1j, to zero.

The determination of the relative timing between the V_{TRANS} and the corresponding V_{IN} time traces is a crucial step in the deduction of the resistive switching time-scales below the duration of the ultra-fast pulses and, thus, has to be carried out at utmost accuracy. Our procedure is based on consistently i) matching the rising edges of the read pulse and of the corresponding LRS response and ii) matching the experimental and simulated LRS and HRS responses to the corresponding V_{IN} signal during the programming pulse. The details of such V_{TRANS} simulations are discussed in Experimental Section.

The high cycle-to-cycle reproducibility of the overlayed ten consecutive periods of V_{IN}, V_{TRANS}(HRS), V_{TRANS}(LRS), and V_{TRANS}(SET) demonstrated in Figure 4 is a key to the enhanced time resolution of the transmitted voltage response: while the sampling rate of the DSO facilitates the acquisition of one data point at every 3.9 ps, the subsequent pulses are sampled at different relative timings due to the period of the V_{IN} cycle which is a non-integer multiple of the instrumental sampling interval. Thus, by overlaying the subsequent pulses, the effective time resolution can be greatly enhanced until the noise limit of the DSO is reached. The enhanced time resolution lies in the heart of our time dependent analysis of V_{TRANS} as it enables the monitoring of <20 ps long resistive switching transitions at the picosecond time-scale. Consequently, throughout the following analysis of the set and reset responses, ten consecutive cycles were overlayed, averaged, and smoothed.

By the optimization of the device layout (see in Experimental Section) a dominantly resistive character of V_{TRANS}(LRS) could be achieved, as evidenced by the perfect overlap between the adequately scaled V_{IN} and V_{TRANS}(LRS) traces in Figure 4a. At the same time, V_{TRANS}(HRS) exhibits an entirely capacitive character corresponding to $C_{MEM} = 3$ fF, while the magnitude of V_{TRANS}(HRS) is kept low. Thereby the desired, high contrast between the reference HRS and LRS responses is established. The excellent agreement between the experimental datapoints (same as in Figure 4a) and the simulated time-dependent transmissions is presented in Figure 4b. Assuming a dielectric constant of $\varepsilon_r = 23$ for Ta_2O_5,[41] the deduced $C_{MEM} = 3$ fF value is a factor of ≈2 higher compared to the prediction of the plate capacitor model taking into account the actual geometrical parameters of our device. We attribute this small difference to the stray capacitance of the electrode and probe arrangements.

Finally, the V_{TRANS}(SET) set switching response (blue, right axis) is compared to the above discussed HRS and LRS reference traces in Figure 4c. A clear transition is observed from the non-switching HRS to the LRS traces within a period which is significantly shorter than the V_{IN} pulse duration. Note, however, that the low C_{MEM} is also crucial in terms of identifying the starting point of the transition: should C_{MEM} moderately exceed 3 fF (our devices), the enhanced first peak of the HRS response would "overshadow" the resistive transition until a relatively low R_{MEM} is reached, that is, the divergence of the V_{TRANS}(HRS) and V_{TRANS}(SET) traces, marked by the blue arrow in Figure 4c, would move to the right. Thereby only the last portion of the resistive transition would remain resolvable. Ultimately, when the influence of a large C_{MEM} becomes dominant in V_{TRANS}(SET), the latter can no longer provide any real-time experimental information on the resistive transition. In the present case, at $C_{MEM} = 3$ fF the first peak of V_{TRANS}(HRS) restricts the resolvable

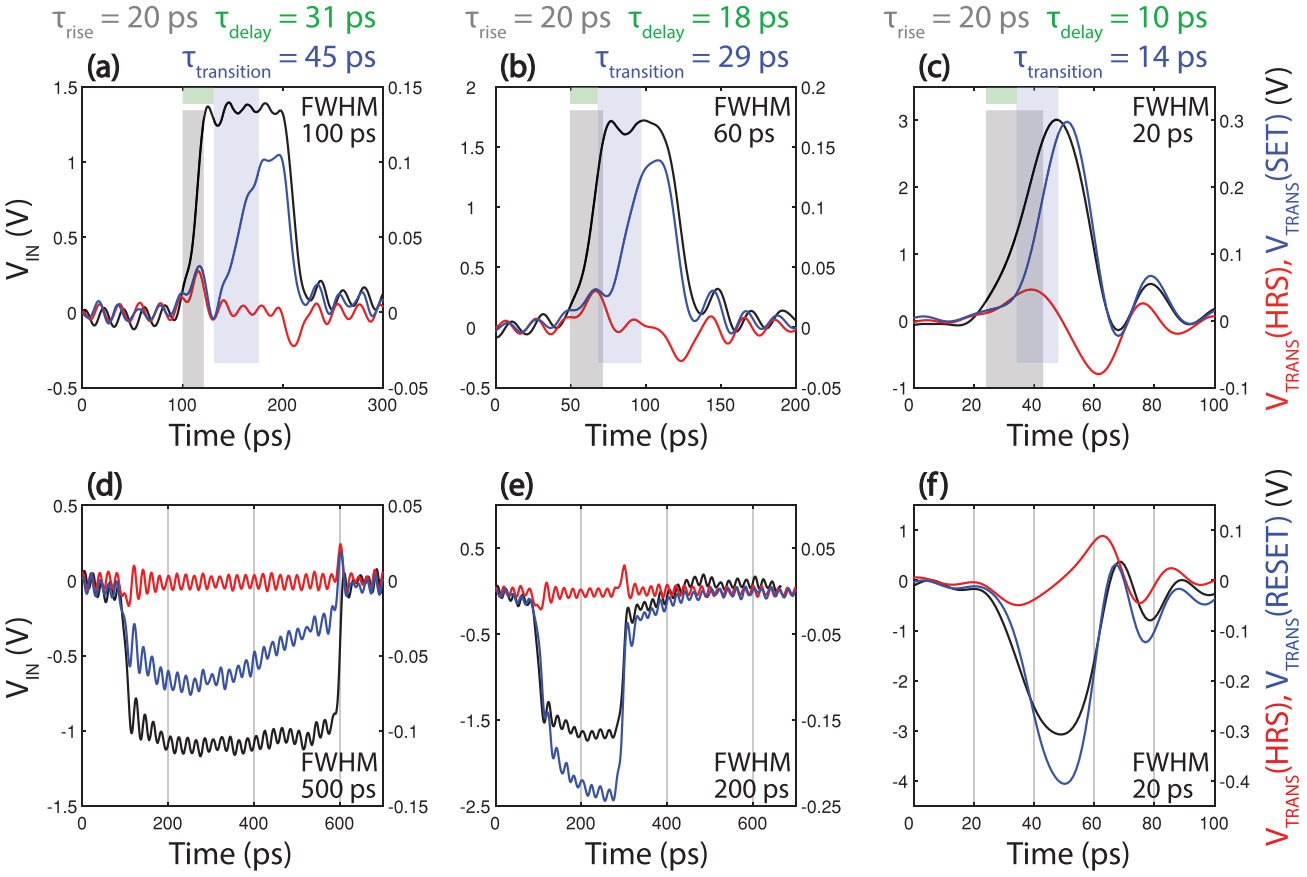

Figure 5. The memristor's resistive response to the fast set and reset pulses are analyzed on the picosecond time-scale. a–c) Magnified view of the time dependence of V_{TRANS} during the 100, 60, and 20 ps long set voltage pulses shown in Figure 2a–c, respectively. d–f) Reset operation due to 500, 200, and 20 ps voltage pulses, respectively. For comparison, the measured, predominantly capacitive transmissions of the HRS corresponding to the actual V_{IN} pulses and C_{MEM} = 3 fF are also plotted (red, right axes). The gray shaded areas in (a–c) highlight the τ_{rise} = 20 ps rise time of the input pulses defined as the time interval between 10% and 90% of the peak value. The blue shaded areas mark the $\tau_{transition}$ time interval of the set switching measured from the apparent divergence of the HRS (red) and switching (blue) traces until 90% of the maximum $V_{TRANS}(SET)/V_{IN}$ ratio is reached. The green shaded areas correspond to the τ_{delay} delay time between the pulse beginning and the onset of resistive switching. The deduced values of τ_{rise}, τ_{delay}, and $\tau_{transition}$ are labeled at the top of the set panels.

resistance change window to $\lesssim$20 kΩ at the shortest available, 20 ps FWHM V_{IN} pulses. Quantitatively corresponding to the noise limitation of our voltage transmission measurement method discussed in Section 2.2, this restriction does not impose any further experimental constraint to our analysis.

2.5. Resistive Switching Time-Scales

Next, we apply the above described approach to resolve the corresponding resistance changes during the programming pulses shown in Figure 2a–f. The magnified views of the corresponding panels are displayed in **Figure 5**a–f, respectively.

The qualitative behavior of the switching trace (blue, right axes) follows a common pattern at each set pulse duration in Figure 5a–c: at the onset of the set pulse (black, left axes) it coincides with the predominantly capacitive HRS response (red trace, right axes) whereas after a transition period it becomes proportional to V_{IN}, as expected for a resistive impedance characteristic to the LRS, in accordance with Equation (1). The time dependence of V_{TRANS} is quantitatively analyzed in terms of the three commonly considered time scales, τ_{rise}, τ_{delay}, and $\tau_{transition}$. The first is an instrumental parameter which is defined between the 10–90% of the set pulse peak and equals to τ_{rise}=20 ± 1 ps, independently of the pulse duration and amplitude, as represented by the gray shaded areas in Figure 5a–c. The blue shaded areas correspond to the $\tau_{transition}$ set transition time. This is defined as the time interval from the apparent divergence of the HRS (red) and switching (blue) traces until 90% of the maximum (resistive) $V_{TRANS}(SET)/V_{IN}$ ratio is reached. Finally, the τ_{delay} delay time is defined as the time interval between the application of the V_{IN} set pulse and the onset of the $V_{TRANS}(SET)$ set switching response, as illustrated by the green boxes in Figure 5a–c. Generally, τ_{delay} accounts for the generation and initial migration of the ionic species contributing to the filament formation.[7,35,42] Due to the finite τ_{rise}, the above definition of τ_{delay} yields to a conservative estimate of the delay time.

The set pulse durations and amplitudes in Figure 5a–c were selected to represent three qualitatively different scenarios. At

the application of a 1.3 V amplitude, 100 ps FWHM set pulse (Figure 5a) the $\tau_{transition}$ = 45 ps long resistive switching starts at τ_{delay} = 31 ps, clearly after the set pulse has reached its plateau. This is the regime where the classical voltage–time dilemma, that is, the exponential acceleration of resistive switching due to a linearly increasing voltage bias applies to the delay time, within the uncertainty imposed by the finite τ_{rise}. At a decreased, 60 ps FWHM but increased, V_{IN} = 1.7 V amplitude set pulse (Figure 5b) τ_{delay} is shortened to 18 ps. Thereby the regimes of τ_{rise} (gray shaded area) and $\tau_{transition}$ (blue shaded area) start to merge, leaving the validity domain of the separately resolvable τ_{delay} and $\tau_{transition}$ time-constants' description behind. Resistive switching again starts around V_{IN} = 1.3 V, however the still rising set voltage and the higher, V_{IN} = 1.7 V plateau result in a faster transition with $\tau_{transition}$ = 29 ps. Ultimately, at a V_{IN} = 3 V, 20 ps FWHM pulse (Figure 5c) the three relevant timescales of τ_{rise}, τ_{delay}, and $\tau_{transition}$ largely overlap, facilitating a constantly accelerating set switching between 1.3 V < V_{IN} < 3 V. The per-definition deduced delay and transition times reach τ_{delay} = 10 ps and $\tau_{transition}$ = 14 ps, respectively.

Below 60 ps FWHM and above V_{IN} = 1.7 V set voltage pulse amplitude τ_{delay} falls below τ_{rise} due to the bandwidth limitation of our AWG, compromising the adopted, common technical definition of τ_{delay}. However, the observation that the resistive transition is consistently triggered at $V_{IN} \approx$ 1.3 V suggests that a pure switching threshold voltage description may have a higher practical relevance in this regime. The $\tau_{transition}$ = 14 ps transition time in Figure 5c corresponds to the ≈65 GHz analog bandwidth bottleneck of our high-speed setup.

Concerning the intrinsic set speed limitations, it is conceivable that the underlying redox and ionic drift processes of the set transition take place at a few interatomic distances around the narrowest cross-section of the conducting filament.[29] They are facilitated by an electric field dependent attempt frequency provided by the vibrational modes of the oxide matrix. The latter are in the order of ≈10^{13} Hz[36,43] rendering the shortest achievable set times to the single-digit picosecond regime. In light of these arguments, we emphasize that, in spite of their instrumental limitations, the experimentally deduced τ_{delay} = 10 ps and $\tau_{transition}$ = 14 ps times approach the ultimate set switching speed limit very closely.

In case of the reset transitions, a closer look at the time dependence of V_{TRANS} in Figure 5d–f reveals a qualitatively different behavior compared to the one of the set switchings. For reference, the non-switching HRS response was also recorded at each programming pulse configuration by adjusting the amplitude of the subsequent set voltage pulses shown in Figure 1j to zero.

The V_{TRANS}(RESET) (blue, right axis) response in Figure 5d is proportional to the V_{IN} (black, left axis) reset pulse of 500 ps FWHM and 1 V amplitude in the first ≈80 ps of the pulse duration, signaling a persisting LRS of resistive character. This is then followed by a slow, ≈320 ps long period of a gradual transition from a resistive to a capacitive response, as seen by the decreasing magnitude and shifting phase of V_{TRANS}(RESET). The phase can be conveniently verified due to the presence of the small amplitude, 50 GHz modulation of V_{IN}. The good quantitative match between the V_{TRANS}(HRS) (red) and V_{TRANS}(RESET) (blue) peaks at 600 ps confirms that the reset transition has been completed within the V_{IN} pulse duration. This behavior, already reported for longer reset pulses,[33] is qualitatively understood in terms of the simultaneous effects of the electric field and the enhanced Joule heating in the LRS: while the former acts to disassemble the conducting filament, the latter assists this destruction by increasing the ionic mobility of the constituting oxygen vacancies.[29] The reset process is then gradually self-terminated by the reduction of the thermal load due to the increasing device resistance.

In contrast, V_{TRANS}(RESET) shows an entirely resistive response without any trace of a capacitive transition during the 200 and 20 ps long reset pulses displayed in Figure 5e,f. As shown in Figure 2e,f, the read pulses of either polarity, applied 10 ns before and after the reset pulse unambiguously and reproducibly confirm the completion of the reset switching also for these two reset pulse configurations. Therefore the above observations imply that the actual reset transition takes place in a delayed manner, after the short reset pulse is over. In order to test this hypothesis, we added a probe pulse of positive polarity, 20 ps FWHM, and 1 V amplitude to the applied V_{IN} scheme, following the falling edge of the reset pulse at different delay times.

2.6. Thermal Reset Delay

A representative reset pump-probe experiment is shown in **Figure 6**a,b, where the probe pulse was fired 200 and 300 ps after the 200 ps FWHM reset pulse, respectively. The device was initialized in similar, R_{LRS} = 2 kΩ and switched to R_{HRS} >

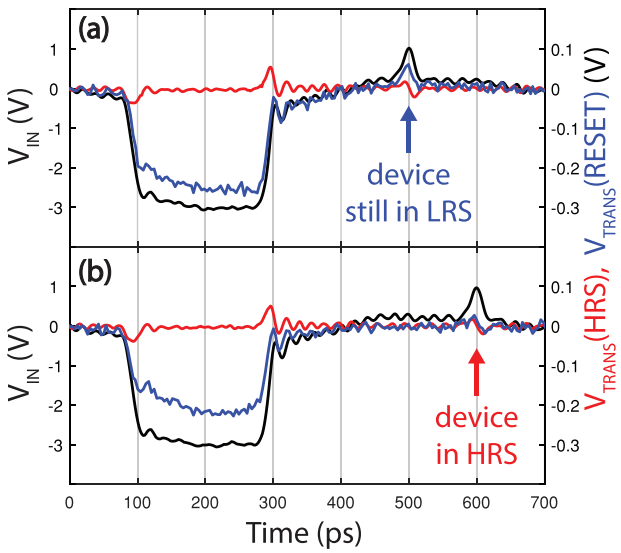

Figure 6. Demonstration of the reset switching delay effect. The V_{TRANS}(RESET) transmission signal (blue, right axes) due to a 200 ps long reset pulse and a subsequent, 20 ps long probe pulse (black, left axes) is shown for different pump-probe pulse delays. The probe pulses, indicated by the arrows, follow the falling edges of the identical reset pulses by 200 and 300 ps in (a,b), respectively. The device was prepared in identical LRS of R_{LRS} = 2 kΩ. For comparison, the simulated capacitive response corresponding to a HRS with R_{MEM} = 100 kΩ and C_{MEM} = 3 fF is also plotted (red, right axes).

20 kΩ according to the 1 ns long read pulses (not shown). The V_{TRANS} response during the reset pulse is entirely resistive in agreement with the previous experiment shown in Figure 5e. The V_{TRANS} response to the probe pulse, however, is markedly different depending on the timing of the latter. The probe pulse following the reset pulse by a 200 ps delay triggers a purely resistive response in Figure 6a, evidencing that the device is still in its LRS. Delaying the probe pulse another 100 ps longer in Figure 6b, on the other hand, results in a capacitive response, in excellent quantitative agreement with the (this time simulated) non-switching HRS transmission corresponding to R_{MEM} = 100 kΩ and C_{MEM} = 3 fF.

These findings demonstrate that the actual reset transition, although can be triggered with programming voltage pulses even as short as 20 ps, needs longer times, in the order of 100 ps, to complete. Importantly, the discovery of the above described reset delay phenomenon also sheds light on the relevant switching mechanism via the temporal separation of electric field and thermally driven effects. The observation that at the time of the reset transition the electric field has already been turned off for 100's of picoseconds provides a solid evidence that the reset process is predominantly driven by the thermally assisted diffusion of the oxygen vacancies constituting to the conducting filament. Meanwhile, the main role of the reset voltage pulse is to establish the high local temperature via injecting the excessive Joule heat in the LRS. The applied electric field is limited by the instrumental bandwidth and pulse power as well as by the break-down durability of the devices. We propose that the time scale of the thermal delay, on the other hand, can be engineered by the careful thermal design of the samples. The latter is a complex task which must take into account the mesoscopic nature of the heat transport at atomically narrow conducting filaments[44,45] as well as the heat capacitance and thermal conduction of the bulk electrodes and their environment. Device miniaturization is expected to facilitate higher local temperatures and, thus, shorter reset time scales at lower reset pulse power. However, fast cyclic operation would also require fast temperature relaxation which is better served by bulkier metallic pathways for more efficient heat removal. The optimization of the above technological aspects must be addressed by further numerical studies.

Time resolved temperature measurements[46,47] as well as continuum models of heat dissipation and conduction[48–50] performed on various nanodevices confirm excess temperatures up to several 100 K as well as decreasing thermal time constants with shrinking active volumes of heat dissipation. Assuming that the heat is released at the scale of the phonon scattering length of ≈10 nm[44] in the metallic LRS of our devices, the reported tendency is consistent with the observed order of 100 ps time-scale. Thermal time constants of this regime have indeed been predicted for redox-based filamentary resistive switching devices also by using continuum model simulations.[43] However, our findings provide the first direct experimental evidence that thermally driven ionic diffusion processes can destruct the conducting filaments and complete the reset transition within this time-scale also in the absence of an electric field.

3. Conclusion

By utilizing current state of the art electronics, we applied fast and uninterrupted, alternating polarity voltage pulse trains down to 20 ps FWHM to facilitate resistive switchings with high cycle-to-cycle reproducibility in Ta_2O_5 based filamentary resistive switches. Resistive switchings and multilevel programming due to 20 ps FWHM set and reset pulses were confirmed by the evaluation of the steady states before and after the programming pulses. The voltage–time dilemma was also revealed in the sub-100 ps time domain. More importantly, our further analysis was focused on the time dependence of the transmitted voltage at the time-scale of the programming pulses. By the optimization of the device layout, we have shown that the capacitive contribution to the transmission can be sufficiently suppressed even at the fastest bias change rates. This enabled the direct, quantitative comparison of the time dependent transmissions corresponding to the resistive switching transition and to the non-switching HRS and LRS reference states at picosecond time resolution. Thereby we have experimentally demonstrated set delay times below 10 ps and set transition times down to 14 ps. The former was instrumentally limited by the finite rise time of our voltage pulse generator, whereas the latter by the analog bandwidth of the detector setup. Nevertheless, we argue that the above values are only a decade away from the ultimate set switching speed limit.

We have shown that reset switchings can also be reliably triggered by 20 ps FWHM voltage pulses in $Ta/Ta_2O_5/Pt$ memristors. However, our pump-probe experiments and the related time dependent analysis also revealed that the duration of the applied reset voltage pulse must not be confused with the actual reset switching time, as the reset process can take an order of magnitude longer time after the ultra-short electrical excitation has been terminated. Such a thermal delay effect, first reported here, provides a strong experimental evidence that the leading mechanism of valence change type reset switching is the Joule heating induced thermal diffusion of the oxygen vacancies which can carry on the reset transition also in the absence of an electric field.

Our results underline the importance of the dedicated thermal optimization of the electrode arrangements terminating atomic scale resistive switches for applications requiring their fast cyclic operation. If the reset times are thereby successfully matched with the picosecond-scale set times demonstrated in this work, VCM based filamentary switches can be readily integrated as high-bandwidth, low-power components into state of the art telecommunication technologies and beyond.

4. Experimental Section

Sample Fabrication: The Pt bottom electrodes, the Au terminals of the co-planar waveguide structure and their Ti adhesive layers were deposited by standard electron beam evaporation at a base pressure of 10^{-7} mbar at a rate of 0.1 nm s^{-1}. The 5 nm thick Ta_2O_5 layers were deposited by reactive high-power impulse magnetron sputtering (HiPIMS) using a Ta target at 6 mTorr pressure, 45 sccm Ar, and 5 sccm O_2 flow rates and 250 W RF power. The stoichiometric composition and the layer thickness were confirmed by XPS spectroscopy. In order

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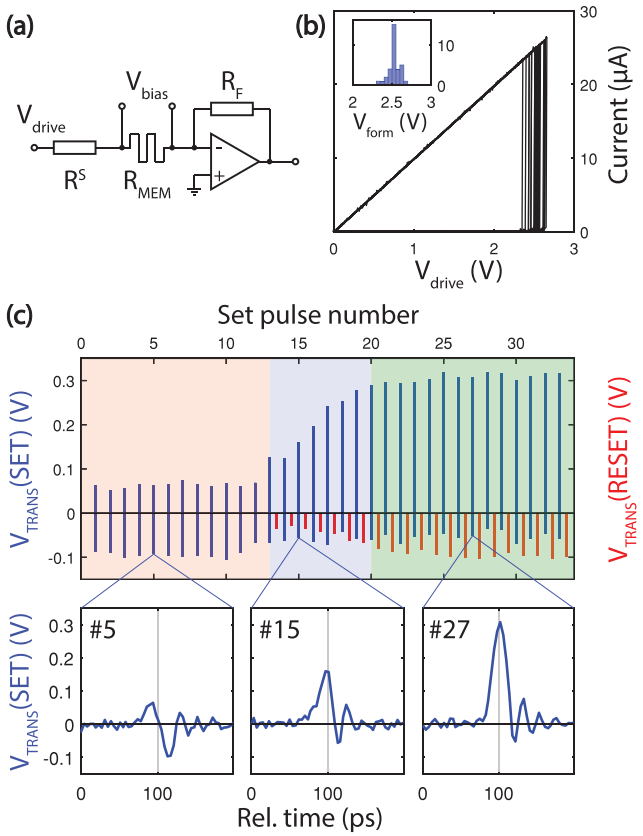

Figure 7. DC characterization setup and electroforming procedures. a) Schematics of the $I(V)$ measurement setup consisting of a series resistor R^S, the memristor device, and a current amplifier. b) DC electroforming traces of 33 devices recorded with $R^S = 100$ kΩ limiting the device current. The inset shows the distribution of the forming voltage. c) An exemplary time series of the schematically represented V_{TRANS}(SET) (blue) and V_{TRANS}(RESET) (red) response pulses as a pristine sample is exposed to 20 ps FWHM and 3.4 V amplitude set as well as 500 ps FWHM and 1 V amplitude reset pulses according to the scheme of Figure 1j. The blue and red lines indicate the measured minimum and maximum values of the V_{TRANS}(SET) and V_{TRANS}(RESET) pulses, respectively. The response to the read pulses and the baseline between the pulses are not shown for clarity. The shaded areas from left to right mark the pristine capacitive response regime (red), the transition from the capacitive to switching response where electroforming gradually takes place due to multiple set pulses (blue) and the established set/reset operations (green), respectively. An inset to each regime illustrates the evolution of the measured V_{TRANS}(SET) pulse shape at a magnified time scale.

to prevent the formation of an ill-defined native oxide at the Ta_2O_5/Ta interface, the Ta electrode and its Pt cap were patterned and sputtered on top of the Ta_2O_5 film at 4 mTorr pressure, 45 sccm Ar flow, and 250 W RF power (125 W dc power) for Ta (Pt).

DC Characterization: The setup of the dc $I(V)$ measurements is shown in **Figure 7**a. The V_{drive} triangular voltage signal was applied on the memristor sample and the series resistor R^S by an NI USB-6341 data acquisition unit (DAQ). The current was measured by a Femto DHPCA-100 current amplifier and the analog voltage input of the DAQ. The V_{bias} voltage drop on the memristor was calculated as $V_{bias} = V_{drive} - I \times R^S$. During DC electroforming $R^S = 100$ kΩ and a 100 mV s^{-1} voltage sweep rate were applied. The 10 kSa s^{-1} data acquisition frequency and the real-time current feedback prevented excess current loads above 20 – 30 μA. The electroforming traces of 33 devices along with the narrow distribution of the deduced V_{Form} forming voltage values are shown in Figure 7b and its inset, respectively, demonstrating high device-to-device uniformity. Following the above electroforming procedure, the hysteretic $I(V)$ traces were recorded by exposing the memristor and an $R^S = 1$ kΩ series resistor to slow (f=1 Hz) triangular V_{drive} voltage signals.

Electroforming by Short Voltage Pulses: The pristine sample was exposed to the repeated pulse sequence shown in Figure 1j starting from a low (<2 V) set pulse amplitude. The latter was gradually increased between the sequences in increments of 0.2 V while the reset and read pulses remained unchanged. Electroforming typically occurred in the set voltage amplitude regime of 2.8 – 4.0 V in a step-by-step manner, as demonstrated in Figure 7c for 20 ps FWHM and 3.4 V amplitude set pulse settings. As illustrated in the insets of Figure 7c, the initial, purely capacitive, non-switching response corresponding to the pristine state gradually transformed into a capacitive-to-resistive switching line shape within 5 – 10 pulsing cycles. Throughout the rest of the pulse train

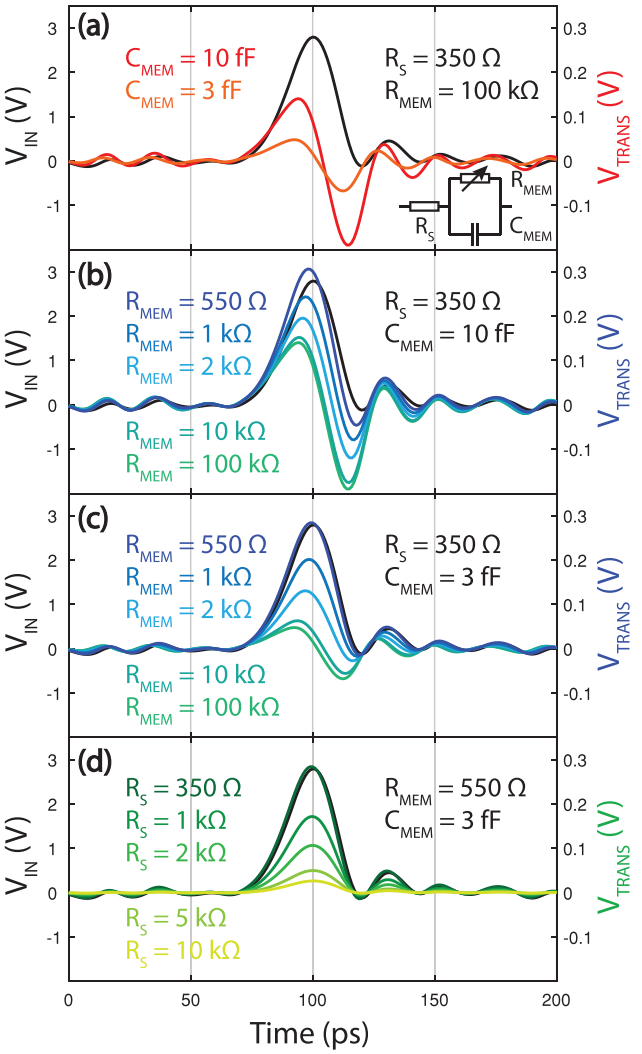

Figure 8. Simulated V_{TRANS} traces for a measured V_{IN} voltage pulse of 20 ps FWHM at various values of the model circuit parameters shown in Figure 1h and also in the inset of (a). The running parameter values indicated to the left of the pulses are displayed in the order of the corresponding traces from top to bottom in each panel. The fixed parameter values are shown on the right-hand side. a) The effect of the device's parallel capacitance on the HRS response. b,c) The effect of the R_{MEM} memristor resistance at $C_{MEM} = 10$ fF and $C_{MEM} = 3$ fF, respectively. d) The effect of the R_S series resistance on the LRS response at $C_{MEM} = 3$ fF.

reproducible set/reset operation was observed between well-established HRS and LRS states, evidenced by the saturation of the V_{TRANS}(SET) and V_{TRANS}(RESET) pulse amplitudes.

Transmission Simulations and Sample Layout Considerations: In order to understand the influence of the individual circuit parameters on the V_{TRANS} response during the ultra-fast voltage pulses, transmission simulations were carried out in LTspice using lossless transmission lines, the equivalent circuit shown in Figure 1h and the measured, 20 ps FWHM V_{IN} pulses. **Figure 8**a shows the influence of C_{MEM} on the HRS response, represented by R_{MEM} = 100 kΩ. The R_S = 350 Ω series resistance value was experimentally determined by measuring reference samples lacking the Ta_2O_5 switching oxide layer. The two red traces corresponding to C_{MEM} = 3 fF and C_{MEM} = 10 fF parallel capacitances illustrates the rapidly increasing capacitive character of V_{TRANS} at C_{MEM} values expected from devices exhibiting sub-micron scale active areas. The decisive impact of C_{MEM} is further emphasized in Figure 8b,c, where the blue traces span over the same R_{MEM} = 0.55 – 100 kΩ range at C_{MEM} = 10 fF and C_{MEM} = 3 fF, respectively. This quantitative comparison demonstrates how the pronounced capacitive contribution to V_{TRANS} could compromise the experimental resolution of R_{MEM} during the pulse, unless C_{MEM} is carefully minimized. Finally, Figure 8d underlines that the latter optimization procedure cannot be implemented simply by the aggressive downscaling of the electrode widths, as the resulting increase of R_S is also detrimental for the real-time resolution of R_{MEM} during the ultra-fast voltage pulses. Based on the above conclusions, the layout shown in Figure 1f,g was implemented intuitively, where the active area of the memristor device was confined at the sub-200 nm scale but the narrow section of the leads was also minimized to a 1 µm distance on either side. The latter feature provided the trade-off between an acceptably low series resistance and a moderate in-plane environmental capacitance. The co-planar waveguide design adopted the structure outlined in ref. [25].

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

M.C. conceived the idea of the project with inputs from A.H, I.S., J.L., and U.K. The samples were fabricated by M.C. with contributions from N.J.O. The high-speed experiments were carried out by M.C. with contributions from Y.H. The data was analyzed by M.C. and was discussed with all authors. All authors contributed to the writing of the manuscript.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

conducting filaments, memristors, picosecond resistive switching, tantalum-pentoxide, thermal reset delay

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