Finite element simulations of graphene based three-terminal nanojunction rectifiers

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Electrical rectification in graphene-based three-terminal nanojunctions is simulated using the finite element method. The model is based on diffusive charge carrier transport in a field-effect transistor configuration. The influence of device geometry, temperature, and electric potential disorder on the rectification efficiency is calculated. For a typical realistic device on a Si/SiO₂ substrate, the model yields a room temperature efficiency of about 1% at a bias of 100 mV. The calculations are compared to previously published experimental results. © 2013 AIP Publishing LLC.

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I. INTRODUCTION

Among the growing number of nanoscale electronic devices, three-terminal junctions (TTJs) built on high mobility materials are promising for high-frequency applications at room temperature. Their non-linear electrical output characteristic allows them to be used as rectifiers,^{1–4} triodes,⁵ frequency multipliers,^{6,7} mixers,^{7,8} and detectors.^{7,8} Furthermore, novel compact devices based on TTJs were demonstrated to work as logic NAND⁵ and NOR gates,⁹ set-reset latch,¹⁰ and half adder.¹¹ Monte Carlo simulations predict a functionality of the ballistic devices up to THz frequencies.⁷ The non-linear effect under consideration is voltage rectification. For a symmetric device with opposite input voltages applied to the left and right branches, the output voltage in the central branch follows the negative input voltage. Transport in high mobility TTJ devices is considered to be (quasi-)ballistic and the non-linearity can be described by the Landauer-Büttiker formalism.^{2,12} However, also diffusive devices cause a similar effect.¹³ The rectification was demonstrated for the first time on graphene in Ref. 14. Although several groups have reproduced the rectification,^{15–17} there are still open questions on the data and on the interpretation. Also effects caused by the junction geometry or the disorder in the graphene remain largely unexplored.

Graphene TTJs are typically formed by etching three constrictions in a graphene sheet as sketched in Fig. 1(a). They are characterized by the channel length (L), the channel/constriction width (W), and the angle (θ). The graphene structure lies on an oxidized silicon wafer. Applying a voltage to the substrate (gate voltage V_G) tunes the charge carrier density in the graphene. Graphene can be tuned from n-type to p-type conduction, depending on whether the gate voltage is above or below the charge neutrality point (Dirac point). Under a voltage bias with V_{in} on the left branch

and $-V_{in}$ on the right branch (so-called push-pull fashion), the central voltage (V_{out}) shows a parabolic dependence on V_{in} (Fig. 1(b)). This is the voltage rectification effect for TTJs. The curvature is given by the applied gate voltage.^{14–16} If the gate voltage is tuned to the Dirac point, the output voltage is zero. For higher gate voltages (electron transport), the curvature is negative and for lower voltages (hole transport), the curvature is positive. However, also the opposite curvature was reported.¹⁶

Here we present a diffusive transport model that is able to explain most of these data. Realistic TTJ geometries are simulated and different effects such as temperature, electric fringing fields, and potential disorder are included in the calculations. The simulations are performed with the finite element method (FEM) software package COMSOL MULTIPHYSICS.

II. THEORETICAL MODEL

The theoretical model for graphene field-effect transistors from Ref. 18 is taken as a framework for the simulations in this work.

A graphene TTJ is modeled by a two-dimensional geometry, as shown in Fig. 1. When this TTJ-geometry is described by x-y coordinates, it is possible to define x- and y-dependent physical quantities such as local charge carrier densities and local voltage.

A charge-voltage balance equation is established, in which a change in the gate voltage bias is compensated by two voltage drops. First, a drop in the SiO₂ due to the electrostatic field caused by the induced electrons and holes in the graphene. Second, a shift in Fermi energy from the charge neutrality point in the graphene due to band-bending. The equation reads as follows:

$$V_G - V_{ch} = -\frac{Q_{net}}{C} + \frac{kT}{q}\eta_F \quad (1)$$

with

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FIG. 1. Illustration of a graphene TTTJ geometry (a) and a sketch of the rectification effect under push-pull voltage bias (b). Depending on the applied gate voltage V_G the output voltage is either always negative ($V_G > V_D$), positive ($V_G < V_D$), or zero ($V_G = V_D$). V_D is the gate voltage at which charge neutrality is achieved in graphene (Dirac voltage). The rectification is symmetric with respect to V_D .

$$\begin{aligned}
 V_{ch} &= -E_F/q, \\
 Q_{net} &= q \cdot (p - n), \\
 p &= N \cdot F_1(-\eta_F), \\
 n &= N \cdot F_1(\eta_F), \\
 N &= 2/\pi(kT/\hbar v_F)^2, \\
 \eta_F &= (E_F - E_D)/kT.
 \end{aligned}$$

V_G is the gate voltage, $V_{ch} = V_{ch}(x, y)$ the local voltage in the graphene sheet (channel), $Q_{net} = Q_{net}(x, y)$ the net mobile charge density in the graphene, $p = p(x, y)$ and $n = n(x, y)$ the hole and electron densities, $E_F = E_F(x, y)$ the Fermi energy in the graphene sheet, F_1 the Fermi-Dirac integral of index 1 (calculated by an approximation given in Ref. 19), $\eta_F = \eta_F(x, y)$ the normalized Fermi-energy with respect to the energy level of charge neutrality or Dirac energy $E_D = E_D(x, y)$, q the elementary charge, k Boltzmann's constant, and $v_F = 10^8$ cm/s the Fermi velocity of the charge carriers.²⁰

$C = C(x, y)$ is the local capacitance per unit area of the graphene sheet. For a parallel plate capacitor model, it is assumed to be constant: $C = C_{ox} = \epsilon\epsilon_0/d$, where ϵ is the dielectric constant of the SiO₂ layer ($\epsilon = 3.9$), ϵ_0 the permittivity of free space, and d the thickness of the dielectric layer ($d = 285$ nm).

Charge conservation in the graphene system yields the static current condition,

$$\nabla \cdot \mathbf{J} = -\nabla \cdot (\sigma \nabla V_{ch}) = 0, \quad (2)$$

where $\mathbf{J} = \mathbf{J}(x, y)$ represents the current density in the graphene sheet and $\sigma = \sigma(x, y)$ the conductivity. As for a conventional semiconductor, σ is assumed to be proportional to the electron and hole concentrations,

$$\sigma = q\mu(n + p), \quad (3)$$

with μ the mobility. It is assumed to be constant and the same for electrons and holes. Note that in this model, the value of the mobility has no influence on the results, as it can be dropped in Eq. (2).

Boundary conditions are a push-pull voltage bias V_{in} on the left structure edge and $-V_{in}$ on the right structure edge, giving a dc-bias to the system (see Fig. 2). The remaining edges have a zero charge condition (i.e., zero normal electric field). For η_F , the boundary condition is zero flux through the graphene edge boundaries.

Breakdown currents for graphene constrictions were reported of the order of a few A/cm² (Refs. 21 and 22). For a monolayer thickness of 0.35 nm, a constriction of 50 nm and assuming a total resistance of 1 k Ω , this gives a maximum voltage bias of about $V_{in} = 100$ mV. Thus, simulations are made for voltage biases below 100 mV.

FIG. 2. TTTJ geometry (colored) on top of a dielectric slab. At the bottom of the slab, the gate voltage is applied. Voltages are applied to the colored left and right edges. The dot in the central branch indicates the voltage probe for the output voltage. The mesh indicates the decomposition of the geometry into finite elements for calculations.

The model does not take into account universal conductance fluctuations, which appear at low temperatures.¹⁴

In summary, the set of Eqs. (1)–(3) with unknowns V_{ch} and η_F is solved over the whole graphene structure. The capacitance C is either constant or a local quantity obtained from 3-dimensional electric field calculations.

III. SIMULATIONS

The simulations are performed on symmetric TJJ geometries as shown in Figs. 1 and 2. We consider junctions with $L = 100$ nm to 500 nm, $W = 50$ nm to 300 nm, and $\theta = 60^\circ$ to 160° . Junctions that are essentially branch-less ($L \approx 10$ nm) are also analyzed. To our estimation, a diffusive model is inappropriate for a TJJ with channel widths below 50 nm, as quantum effects become important in such constrictions (e.g., the opening of a transport gap^{23,24}).

First the results for the two-dimensional (2D) case with $C = C_{ox} = \text{const.}$ are shown, followed by a discussion for the behavior near the Dirac point. Then the pseudo-three-dimensional case is shown, where the fringing effects of the electromagnetic field between the gate electrode and the graphene sheet (giving a local capacitance $C = C(x, y)$) are included in the calculations. In this section, the influence of the TJJ geometry on the rectification efficiency is explored.

Finally, the effect of electric potential disorder is included in the simulations.

A. Plate capacitor approximation (2D-model)

In the 2D model, $C = C_{ox}$ is kept constant. As can be expected from a diffusive model, the TJJ geometry then has no influence on the rectification. All geometries give the same result.

Fig. 3(a) shows the calculated conductivity in a graphene TJJ at 77 K. A bias of 100 mV is applied to the left and -100 mV to the right branch. A positive voltage of $V_G = 0.17$ V is applied to the gate, yielding electron-dominated transport in the device. The left branch is positively biased and so features less electrons than the right branch, which is negatively biased. Thus the conductivity is lower in the left than in the right branch. The asymmetric conductivity distribution throughout the graphene device creates a non-zero voltage in the central branch (Fig. 3(b)). For electron transport, it is negative and for hole transport it is positive.

In Fig. 3(c), the output voltage is plotted versus push-pull input voltage for different temperatures and different positive V_G (electron-dominated transport). For each temperature, the gate voltage giving the best rectification was

FIG. 3. (a) Conductivity $\sigma(x, y)$ and (b) electric potential $V_{ch}(x, y)$ calculated for 77 K, a push-pull bias of $V_{in} = 100$ mV and a gate-voltage of $V_G = 0.17$ V (carrier mobility of $4000 \text{ cm}^2/\text{Vs}$). (c) V_{out} vs. V_{in} and (d) V_{out} vs. V_G curves for different temperatures. Inset in (d) zooms in on the higher temperatures. In (c), each curve corresponds to the gate voltage at which the rectification is highest.

chosen. All curves are parabolic, except for 4 K (see below). Increasing the temperature markedly reduces the rectification efficiency, $|V_{out}/V_{in}|_{V_{in}=100\text{mV}}$: it is 52% at 4 K, 16% at 77 K and 1% at room temperature. For negative V_G (hole dominated transport), the same result is obtained, but with all curves bend upwards.

In Fig. 3(d), the output voltage is calculated for different temperatures over a broad gate voltage range, with a push-pull voltage of $V_{in} = 100\text{mV}$. As no doping of the graphene is considered here, the charge neutrality point is at $V_G = 0\text{V}$. The hole and electron transport regimes are distinguished to its left and right, respectively. V_{out} is positive in the hole regime and negative in the electron regime. Each curve crosses 0 for $V_G = 0\text{V}$ as at the charge neutrality point a symmetric configuration of the same amount of holes in one branch as electrons in the other branch is build up in the graphene channel. This yields the same conductivities left and right and a cancellation of the rectification. Further away from the Dirac point, two maxima (of equal absolute value) can be seen on both sides of it for each curve. For high V_G voltages, all curves approach 0 asymptotically. This is expected, as the high carrier densities in this regime lead to small differences in conductivities in the branches when compared to the overall conductivity. Going down in temperature increases the value of the maxima and moves them closer to the charge neutrality point than in the high temperature case. Increasing temperature leads to increasingly mixed electron and hole contributions to the conductivity, which smears the rectification.

To better illustrate the curve for 4 K in Figure 3(c), several rectification curves are calculated with gate voltages near the Dirac point in Fig. 4. The rectification curves are always nearly parabolic for any gate voltage. But for sufficiently large V_{in} , the curve changes inflexion. For high temperatures, the inflexion happens at very high V_{in} , so that this “transition” is not seen; the parabola effectively flattens down for $V_G \rightarrow 0$.

Generally, increasing V_{in} results in a better rectification. However, when V_G is very close to the charge neutrality point and $V_{in} > V_G$, then the difference in conductivities in the left and right branch is negligible, leading to an ineffective rectification. V_{out} still increases with increasing V_{in} , but less pronounced than in the parabolic regime. For higher temperatures, both electron and hole densities contribute considerably to the conductivity close to the Dirac point. This smearing guarantees a difference in conductivities in the left and right branch and a parabolic rectification is seen at all gate voltages.

B. Influence of the TTJ geometry on the rectification efficiency (pseudo-3D-model)

As the channels of TTJ are small in size compared to the gate area, electric fringing field lines become important. They lead to charge accumulation at the graphene edge and so the plate capacitor model is no longer valid. This is especially relevant if the branch dimensions L and W are comparable to or smaller than the dielectric thickness d . A theoretical analysis of this effect can be found in Refs. 25

and 26. Recently, strong conductance enhancement at the edge of graphene devices was measured by scanning gate microscopy.²⁷

In order to simulate a more realistic graphene rectifier than in Sec. III A, a local capacitance is first calculated between the graphene sheet and the gate electrode in the configuration shown in Fig. 2. The local capacitance is then used to run the simulations on the (two-dimensional) TTJ geometry.

The local capacitances of different TTJs are shown in Fig. 5. For branch-less junctions as seen in Figure 5(a), the fringing field lines are screened by the reservoirs and no distinguishable conductivity enhancement takes place in the channel; the parallel plate capacitor approximation ($C = C_{ox}$) can hold. But at unscreened edges (see Figs. 5(b)–5(d)), an increased charge density can be distinguished. For narrow channels, the contributions from both edges overlap (Figs. 5(c) and 5(d)). Regions more than 500 nm away from the edge can be considered as bulk, where $C = C_{ox}$.

A locally enhanced capacitance implies a higher induced majority charge carrier concentration as well as a lower minority charge carrier concentration in those regions. In consequence, the local conductivity is always enhanced in those regions (see Eq. (3)). This leads to a better rectification, when compared to results in the plate capacitor approximation under the same bias conditions. The effect is more pronounced for junctions with narrow but long branches.

To demonstrate this effect, calculations were performed on the T-junctions with $L = 500\text{nm}$ and widths from $W = 50\text{nm}$ to 300nm at 77 K and 300 K (Fig. 6). The result for the plate capacitor approximation is shown for comparison. Calculations with the local capacitances show an increase in rectification for TTJs with narrow branches. For very narrow branches, the maximum rectification efficiency increases approximately up to a factor 2 at 77 K and 300 K. Also, the V_G value for maximum rectification moves closer to the charge neutrality for narrower branches.

Summarizing, the effect of the fringing fields leads to an enhanced rectification, when compared to the plate capacitor

FIG. 4. Non-parabolic behavior close to Dirac point in the electron transport regime ($V_G > 0$). The dotted curve shows the transition to the hole transport regime ($V_G < 0$).

FIG. 5. Calculated local capacitances for a branch-less junction with $W = 50$ nm (a) and junctions with branches of length $L = 500$ nm and $W = 300$ nm (b), $W = 100$ nm (c), and $W = 50$ nm (d). A high local capacitance implies a high local conductivity.

model. The maximum efficiency is reached at a lower V_G and V_{out} drops to zero quicker for high V_G values.

C. Effect of disorder

Due to sources of disorder electron-hole puddles are found in graphene on SiO_2 .^{28,29} The charge puddles are believed to arise from long-range Coulomb scattering of defects in the substrate and from charged impurities. From experiments, the standard deviation of puddle density n^* is estimated to be $4 \times 10^{10} \text{ cm}^{-2}$ (Ref. 28), $4 \times 10^{11} \text{ cm}^{-2}$ (Ref. 29), and $4.3 \times 10^{11} \text{ cm}^{-2}$ (Ref. 30). The spatial extension of these puddles is reported to be 20–30 nm. They are spread randomly over the graphene sheet. The above experimental findings indicate that the puddle density can have a

considerable effect on the conductivity of graphene devices and should therefore be considered for the calculations.

The overall effect of disorder can be thought of as a modulation of the applied gate voltage acting on the graphene sheet carriers. The puddles are thus modeled by adding a disorder “gate” voltage V^* to the balance equation (1). V^* is chosen to be a periodic potential $V^*(x,y) = A/2 (\sin(q \cdot x) + \sin(q \cdot y))$, with an amplitude of $A = q/C_{ox} \cdot n^*$. The frequency q is chosen to yield puddles with a diameter of about 28 nm.

Calculations are performed on a junction with short branches ($L = 20$ nm) and a constriction width of 200 nm. Figure 7(a) shows $V^*(x,y)$ on the graphene geometry. V^* induces disorder on the normalized Fermi energy η_F^* of the system. The amplitude of $kT\eta_F^*$ close to the Dirac point is denoted Δ . The obtained values of Δ for given A or n^* are

FIG. 6. V_{out} vs. V_G calculated for T-junctions with $L = 500$ nm and widths from $W = 50$ nm to 300 nm at (a) 77 K and (b) 300 K.

FIG. 7. (a) Disorder potential (V^*) on junction with $L = 10$ nm, $W = 200$ nm and $\theta = 120^\circ$. The shown amplitude (A) is 3 V. Calculations are done on this junction with different amplitudes. (b) V_{out} vs. V_{in} and (c) V_{out} vs. V_G at 77 K. In (b), each curve corresponds to the gate voltage at which the rectification is highest.

listed in Table I. Figures 7(b) and 7(c) show the rectification and efficiency curves at 77 K for different disorder potential amplitudes. Increasing the amplitude, decreases the rectification effect.

TABLE I. Correspondence between amplitudes of V^* , n^* , and Δ .

A [V]	n^* [10^{11} cm^{-2}]	Δ [meV]
0	0	0
0.5	0.4	30
1	0.8	50
2	1.5	80
3	2.3	100
5	3.8	130
10	7.6	190

IV. COMPARISON WITH EXPERIMENTAL DATA

In order to compare the simulation results with experimental data from references, we introduce a parameter α . It is the curvature of the V_{out} vs. V_{in} curve in parabolic approximation: $V_{out} = \pm \alpha \cdot V_{in}^2$. The results from this work help to understand the rectification effect found in Ref. 14. The experiments show a curvature of $\alpha = 0.2 \text{ V}^{-1}$ at 77 K at a gate voltage approximately 3 V away from the Dirac point. The simulations show that this is possible when disorder in the range $\Delta = 100$ –130 meV is used (see Fig. 7(c)). At room temperature, the experiment shows a curvature of $\alpha = 0.1 \text{ V}^{-1}$ at a gate voltage approximately 5 V away from the Dirac point. This is seen in the simulations for the same disorder range. The rectification efficiency reaches 50% at 4 K in the model (corresponding to $\alpha \approx 5 \text{ V}^{-1}$). At this temperature, universal conductance fluctuations dominate the

electronic transport properties. Their presence weakens the rectification effect. The experiments show a curvature of $\alpha = 0.3$ to 0.4 V^{-1} .

Another reported graphene-based TJJ on Si/SiO₂¹⁵ shows a similar output characteristics as found in Fig. 3. The maximum curvature at room temperature is $\alpha = 1.8 \text{ V}^{-1}$, which is about 20 times higher than in Ref. 14. This is explained by contributions of ballistic transport to the rectification, as the mobility is three times higher than in Ref. 14. The proposed lumped circuit model can be derived from Eq. (1) when the temperature is zero. It is in agreement with the data for high gate voltage but breaks down for gate voltages around the Dirac point, where it predicts a diverging output voltage.

V. CONCLUSION

The diffusive transport model presented in this paper describes well the basic mechanisms of the rectification effect in graphene-based three-terminal nanojunctions. According to the model, the rectification efficiency is decreased by an order of magnitude when increasing the temperature from 77 K to 300 K. Also the geometry of the devices is shown to affect the efficiency. Narrower and longer branches can enhance the efficiency by a factor of 2. Furthermore, the model shows that typical potential disorder present in graphene devices on SiO₂ weakens the efficiency by a factor of 10 at 77 K and by a factor of 2 at 300 K. A maximum room temperature efficiency of only about 1% is obtained in the calculations. The data from Ref. 14 can be described with this model.

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