Caliste-SO: The X-ray Spectrometer Unit of the STIX instrument onboard the Solar Orbiter space mission

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ABSTRACT

Caliste-SO is a hybrid detector integrating in a volume of $12 \times 14 \times 18 \text{ mm}^3$ a 1 mm-thick CdTe pixel detector, a front-end IDeF-X HD ASIC and passive parts to perform high resolution spectroscopy in the 4-200 keV energy range with high count rate capability (10^4 - 10^5 photons/s/cm²). The detector hybridization concept was designed by CEA and 3D-Plus to realize CdTe cameras for space astronomy missions with various pixel patterns. For the STIX instrument onboard the Solar Orbiter mission, the imaging system is made by 32 collimators that sample the visibilities of the spatial Fourier transform and doesn't require fine pitch pixels. The Al-Schottky CdTe detectors produced by Acrorad are then patterned and tested by the Paul Scherrer Institute to produce 12 pixels surrounded by a guard ring within 1 cm². Electrical and spectroscopic performance tests of the Caliste-SO samples are performed in France at key manufacturing steps, before sending the samples to the principal investigator to mount them in the Detector Electronics Module of STIX in front of each collimator. Four samples were produced in 2013 to be part of the STIX engineering model. Best pixels show an energy resolution of 0.7 keV FWHM at 6 keV (1 keV resolution requirement for STIX) and a low-level detection threshold below 3 keV (4 keV requirement for STIX). The paper describes the design and the production of Caliste-SO and focuses on main performance tests performed so far to characterize the spectrometer unit.

Keywords: CdTe, front-end ASIC, X-ray spectroscopy, Fourier telescope, solar flares.

1. INTRODUCTION

1.1 Telescope overview

The Spectrometer Telescope Imaging X-rays (STIX) is part of the suite of remote sensing and in-situ instruments onboard the Solar Orbiter mission adopted by ESA in 2011 to be launched in 2017 [1]. The time-resolved imaging spectroscopy of solar flares in the hard X-ray range (4-150 keV) will give information about the intensity, the location and the energy of electrons accelerated in the heliosphere. The 7 arcsec angular resolution can be achieved at perihelion by a Fourier imaging technique, consisting in measuring the Fourier complex visibilities of the image using non rotating collimators made of grid pairs. The imager of STIX is composed of 30 collimators whose grids have a variety of slit spacings and orientations to sample the (u,v) plan of spatial frequencies at a variety of points, plus 2 collimators for Sun coarse location (pinhole system) and background evaluation (opaque system). In the Detector Electronics Module (DEM) underneath the imager tube, X-ray photons are then detected and events are processed to obtain on-board light curves, spectra and visibility measurements. The time resolution of the images is limited by the photon statistics and can

be as low as 0.1 s for very bright events. A 4 arcsec pointing accuracy can be obtained using an aspect system made of a lens, a series of holes and photodiodes in the center part of the telescope to precisely measure the position of the solar limb with respect to the telescope optical axis. The telescope is protected from thermal load and straylight by X-ray windows placed in front of the imager in the feedthrough of the spacecraft. Figure 1 is a 3D view of the STIX instrument showing the subsystems and their volume allocation to achieve a 6 cm² effective area. The current design is 7 kg mass, 6 W electrical power in normal operation mode and 8 W in case of intense solar flares.

Figure 1. Overview of the STIX instrument on board Solar Orbiter.

1.2 Specifications of the detection unit

The front-end board of the DEM includes 32 detection units aligned behind each collimator of the imager to perform photon-counting and spectroscopy in the hard X-ray range. The front grid and the rear grid of one collimator are slightly twisted with respect to each other to create a Moire pattern on the detector. In this manner, a coarse pixelating of the sensor to measure this pattern gives access to the real and imaginary parts of the Fourier complex visibility [2]. The scientific and technical requirements for an elementary detection unit are stated in Table 1.

Table 1. Requirements for one detection unit of the STIX instrument.

Parameter	Requirements
Energy range	4-150 keV
Count rate capability	50 % detection efficiency at 100 keV 2.10 ⁴ counts/s (goal 10 ⁵)
Energy resolution	1 keV FWHM @ 6 keV 15 keV FWHM @ 150 keV
Detection surface	1 cm ²
Electrode pattern	4 bands or higher pixelating
Power consumption	20 mW

CEA Saclay is responsible for the design and the fabrication of the detection units of STIX. The device Caliste-SO was developed for this purpose. Section 2 presents the concept of this technology and defines the subsystems. Section 3 describes the fabrication flow including tests and illustrates the current realizations for the project. Section 4 presents the performance results obtained with the first samples.

2. CALISTE-SO DEFINITION

2.1 Introduction to Caliste-SO design

Caliste-SO is a CdTe hybrid detector based on R&D for high energy astronomy space experiments. Cadmium telluride is a semiconductor detector that provides a number of advantages for X and gamma-ray spectroscopy. The high density and

high atomic number allow high detection efficiency in the hard X-ray range with thin layers (99 % total detection efficiency at 50 keV and 62 % at 100 keV with 1 mm thickness). Schottky-type metal contacts result in diode detectors with very low leakage current at room temperature (2-5 nA/cm² @-300V, 6-10 nA/cm² @-600V) and provides excellent spectrometers with moderate cooling (no need for cryogenics on the contrary to Germanium detectors used in RHESSI [2]). For an instrument with very limited resources in power and volume, both features are very attractive. Such detectors will be used prior to Solar Orbiter for the Hard X-ray Imager and the Soft Gamma-ray Camera of the Japanese Astro-H mission for high energy astronomy to be flown in 2015. For STIX, the 1 cm² CdTe detectors are patterned in 4 bands surrounded by a 300 μ m guard ring to limit leakage current in the pixels due to surface defects at the crystal periphery. Each band is subdivided in two large pixels and one 'button' pixel as illustrated in Figure 2. The segmentation in two large pixels introduces redundancy in the measurement of the visibility (which can be used to correct from position accuracy with respect to the grids for instance) and reduces the leakage current and the input capacitance of the analog channel (which are the 2 key parameters to optimize electronic noise and thus spectral resolution). The button pixels are used to get better estimates of the spectral response and the photon counts in case of bright events (little probability of pile-up events in these small areas).

Figure 2: (a) Simulation of photons impinging the detector after going through the two grids of the collimator. The phase and amplitude of the Moire pattern (and thus the complex Fourier visibility) can be obtained by measuring the total counts in four bands of the detector. (b) Pixel pattern of the 10 mm $\times$ 10 mm Schottky anode of the CdTe detectors in STIX.

Figure 3: Caliste-SO CdTe hybrid detector overview (a), with details on the inner part of the electrical body (b).

Caliste-SO is the hybridization of this CdTe pixel sensor with a so-called electrical body based on 3D Plus technology. The Caliste-SO body includes 4 mini printed circuit boards placed perpendicular to the detection surface and molded in an epoxy resin, as shown in Figure 3b. One PCB holds the front-end ASIC called IDeF-X HD designed by CEA. 13

2.3 Caliste-SO implementation in STIX

The Detector Electronics Module is divided into two parts. The detector front-end box includes cold electronics (the Caliste-SO units, analog buffers, filters and temperature sensors connected to a cold element at -20°C) and warm front-end electronics (analog-to-digital converters, voltage regulators, test pulse generator, filters possibly at $+50^{\circ}\text{C}$). The instrument data processing unit includes power supply units, FPGAs to control the Caliste-SO units (configuration and event readout) and all ADC (for aspect system photodiode, temperature and photon energy signal encoding), and flight application software for scientific data processing and Spacewire communication with the spacecraft.

Caliste-SO is a self-triggered system. When an event is detected, i.e. when the signal in one analog channel of the ASIC at least reaches the low-level threshold, the controller starts a readout sequence to get the position and the energy of the photon interaction. During the phase that can last from 5 to 20 μs according to readout parameter settings, the full device is blind to new incoming photons. The slow control protocol of IDeF-X HD allows connecting up to 8 ASICs together with a complete I/O signal sharing. In STIX, the Caliste-SO are grouped by 2, as a compromise between electrical interface reduction and availability for high rate counting. The 16 groups of Caliste-SO are processed independently with their own ADC.

3. CALISTE-SO FABRICATION AND TESTS

3.1 CdTe sensor fabrication and tests

Each sensor of $10 \times 10 \times 1 \text{ mm}^3$ is cutted out from CdTe dies of $14 \times 14 \times 1 \text{ mm}^3$ in size provided by the Acrorad company. A microfabrication process was developed at the laboratory of micro and nanotechnology of the Paul Scherrer Institute (PSI LMN) to create pixels plus guard ring out of by the CdTe supplier predeposited anode (Al/Ti/Au multilayer). The fabrication flow consists of photolithography, plasma etching, dicing and cleaning. Leakage current measurements are performed by PSI at $+20^{\circ}\text{C}$ and -20°C on each individual pixel in order to select sensors with lowest dark currents and to confirm the correct operation of the pixels. The in-house developed dark current measurements set-up allows the installation of four CdTe pixel detectors in parallel into the vacuum chamber. All detectors are cooled by a coolfinger directly attached to the detector cathode contact. A close-up of the test board is shown in Figure 5. The system can measure currents with a precision better than 1 pA.

Figure 5: Test set-ups for dark current measurement of CdTe pixel sensors. (a) The pixelated anode is pressed against individual soft electrical contacts and the planar cathode is in electrical contact with the high voltage signal. (b) The board inside the thermal chamber is equipped with a series of relays to alternatively connect and disconnect the pixels to the ammeter.

Another test setup has been developed by ETH Zurich and PSI for spectroscopy measurements. The similar holding system for the CdTe pixel sensor is connected to an ASIC board and a full acquisition system is installed in the clean room to record ^{133}Ba spectra at -20°C . Good crystals are delivered to 3D Plus for mounting on top the Caliste-SO bodies.

3.2 Hybrid fabrication and tests

To fabricate the Caliste-SO device, the first step consists in mounting and bonding the bare ASIC on a PCB and brazing flying leads for pixel connection; functional and performance tests are performed on the ASIC PCB at room temperature. The other PCBs are fabricated and undergo electrical continuity tests. The four PCBs are stacked and molded in an epoxy resin; the resulting block is cut and metallized with a thin Ni-Cu-Ni-Au layer; lateral routing is then performed by laser ablation. The bottom interface with the small outline package is added. The copper link is covered with a Ni/Au layer and glued to the Caliste-SO Body. The top surface of the block is then prepared to have connection areas for detector electrodes and high voltage signal. These areas are in contact with the flying leads. Each Caliste-SO Body is tested at 3 temperatures with a test injection signal in the thermal chamber shown in Figure 6. The CdTe detector is then mounted on top of the Caliste-SO body using a special flip-chip process based on polymer bump bonding technique. The high voltage is connected to the detector according to a special wire-bonding process adapted to CdTe detectors. The full device undergoes electrical characterizations and spectroscopic acceptance tests in France with the same test set-up as in Figure 6 and is exported to Switzerland for calibration and integration in STIX.

Figure 6: Test set-ups for electrical tests of Caliste-SO bodies and Caliste-SO by 3D Plus and spectroscopic tests of Caliste-SO complete devices by CEA. Up to 8 devices can be cooled down and tested in parallel with temporary electrical connections.

3.3 Space qualification

The two specificities of space environment are the mechanical and thermal conditions during launch (vibrations, shocks, pressure and temperature variations on mechanical parts) and the radiation environment during the mission (total ionizing dose effects and displacement damage in semiconductors). The 2 parts that are not space qualified in Caliste-SO are the front-end ASIC and the CdTe pixel sensor. IDeF-X HD will follow the classical process of space qualification for an electrical component. Preliminary characterization tests related to radiation hardness are presented in paragraph 4.4. Main concerns about Solar Orbiter radiation environment is related the effect of the proton flux on the CdTe detectors (10^{11} protons/cm 2 expected after 10 year mission). A test campaign with 50 MeV protons was set up with samples of CdTe pixel sensors. Gain loss and energy resolution are visible due to defect accumulation in the semiconductor. Characterizations of the irradiated samples and result interpretation are on-going.

Most materials and processes used in Caliste-SO are part of 3D Plus product identifier (PID) certified by ESA. A qualification plan was built with the support of CNES and successfully lead to validate processes out of 3D Plus PID in Caliste-SO bodies, as well as the detector interface process and the high voltage connection process. To conclude on the

compliance of Caliste-SO hybrid technology and its mounting process in STIX, a quarter of the STIX qualification model will be equipped with Caliste-SO samples and will undergo thermal and vibration tests.

3.4 First production batches

In implementation phase, two production batches of 4 samples each were produced. The prototypes were built to validate the design concept (see Figure 7b). Individual current measurements on CdTe sensors were not available at that time. Best energy resolutions obtained at -30°C were 0.8 keV FWHM at 14 keV with a button pixel and 1.15 keV FWHM with a large pixel. But some pixels were not functional, most probably due to an excess of surface leakage current. The pattern process was then improved in PSI; new samples were produced and tested with the set-up of Figure 5 for the following Caliste-SO batch (see Figure 7a). Dark current performance is illustrated in paragraph 4.1. The next Caliste-SO bodies produced showed small defects: the channel connected to the guard ring was nonfunctional and the electrical insulation of the high voltage signal inside the body was not sufficient. As a result, the Caliste-SO engineering models are operated with high voltage amplitude not higher than 100V. Spectral performance is presented in paragraph 4.2. The design of the body and the process of top surface preparation were revised. A new batch is currently in production and samples no longer show the defects on the high voltage and the guard ring. First complete devices of this batch will be ready mid-2014 and will partly equip the qualification model of STIX.

Figure 7: (a) CdTe Schottky anode to flip chip on a Caliste-SO body. (b) First complete Caliste-SO prototype device.

4. CALISTE-SO PERFORMANCE CHARACTERIZATION

4.1 Dark current measurements

Figure 8 shows leakage current measurements performed with the set-up of Figure 5 on a detector sample that was later on mounted on a Caliste-SO engineering model. One measurement cycle including chamber pump down time, detector cooling to -20°C and detector loading lasts around 8 hours. For the correct and low noise operation of the Caliste-SO detector module, the pixel leakage current must not exceed 62 pA under 300V bias. The flowing dark current in the guard ring doesn't contribute to the spectrum and is therefore insignificant although connected to one of the input channels of the ASIC. The yield of fabricated pixel detectors in terms of current requirement is $\sim 85\%$. Pixel currents as low as 25 pA in a large pixel and 3 pA in a small pixel can be obtained in these conditions.

4.2 Spectral performance

Spectroscopy measurements were performed on Caliste-SO engineering models with the set-up of Figure 6. For each Caliste-SO sample, pixel spectra are individually calibrated and histograms are summed up to obtain the Figure 9. Energy resolutions of 0.7 keV and 1.0 keV FWHM at 14 keV were respectively obtained on the sum spectrum of the button and the large pixels, when the device is cooled down at the STIX nominal operating temperature of -20°C . The low-level threshold can be set in the best case as low as 2 keV for the button pixels and 3 keV for the large pixels without noise peak. The left tailing of the 60 keV line reveals some charge loss in the CdTe detector due to a rather low electrical field and should be almost suppressed in the next production batch when applying a higher bias voltage. The main advantage of this hybrid design using 3D integration is to minimize the input capacitance of the ASIC which influences at most the noise performance for a short shaping time. From various spectral measurements with Caliste-SO

and knowing the properties of IDeF-X HD ASIC, we evaluated the detector capacitance plus the stray capacitance to be ~ 2 pF for the button pixels and ~ 3 pF in the large pixels. As a result, equivalent noise charge as low as 100 electrons rms can be obtained with 9 mm^2 pixels with rather fast timing signal integration ($2 \mu\text{s}$). This allows reaching simultaneously high spectral performance and high counting capabilities.

Figure 8: (a) Dark current measured at $+20^\circ\text{C}$ (a) and at -20°C (b) on the 12 pixels and the guard ring of the CdTe pixel detector for the Caliste-SO engineering model #1. The Schottky diode is backward biased at -300V to obtain very low leakage current and good spectral performance.

Figure 9: ^{241}Am spectra with the Caliste-SO engineering model #1 cooled down to -20°C , biased at -100V ($6 \mu\text{s}$ shaping time). Energy resolution is measured at 14 keV (FWHM1) and at 60 keV (FWHM2). Energy resolution is visibly better for the button pixels because they have 10 times less leakage current and 1 pF less input capacitance than the large pixels.

4.3 Count rate capabilities

A software simulator of Caliste-SO was implemented by modeling the responses of the CdTe semiconductor detector, the front-end ASIC and the readout electronics. An event is defined by a time of arrival, an absorbed energy, a pixel number, a status flag and a readout energy. One photon can create several events in case of X-ray fluorescence or charge sharing between pixels. Times of arrival are generated according to a Poisson law distribution with a mean count rate parameter defined by the user. Absorbed energies are computed using a Geant 4 model of the detector and the photon source (no simulation of the collimator grids). The pixel number is determined from a basic model of signal induction in CdTe assuming no charge loss or charge cloud diffusion. For each event time, the ASIC trigger time depends on the low-level threshold, the shaping time and the signal amplitude and is computed from simulation results obtained with the Cadence design tool. From the trigger time, the controller waits during a so-called latency time so that the Gaussian pulse at the filter output of the analog channel reaches its maximum value. An event that occurs in the latency time in a pixel already hit is flagged as 'pile-up'. The pile-up fraction is the number of pile-up flags out of absorbed photons. In STIX, only the energies of the single-hit events are read out. The throughput is this fraction of processed events. At low rate, the throughput depends on the fraction of the single events defined by the matrix geometry (fraction of pixel area and inter-pixel area); at medium rate matrix geometry only depends on the dead time of the readout sequence and the matrix geometry (determining the fraction of single events). At high rate, the throughput decreases because events are missed during the readout sequence (dead time) but also because events occurring in 2 pixels of the Caliste group in the same latency time window are not processed. Figure 10 illustrates timing results of a simulation for one typically readout configuration and various source count rates. At 20000 cts/s/cm² rate (STIX baseline), pile-up fraction is 0.2% and throughput is 62 % (90 % of the throughput at low rate). The simulator can also be used to study the spectral deformation in high rate conditions since it precisely computes the energies stored in the peak detectors assuming a Gaussian shape pulse, in particular in case of pile-up.

Figure 10: Simulation in case of a uniform illumination of the CdTe matrix by a 10 keV photon source and a configuration close to STIX conservative parameters (group of 2 Caliste-SO units, single event read out mode, 3 keV threshold for all pixels, guard ring disabled, 2.5 μ s latency time, 10 μ s readout time). (a) Fraction of pile-up events during the latency time and missed events during the readout time. (b) Throughput in numbers of triggers (all event multiplicity) and processed events for STIX (single events only).

Impact of high rate conditions on spectral response was experimentally studied on one Caliste-SO engineering model with a ⁵⁷Co source up to 9000 cts/s/cm². Gain, offset, energy resolution at 14 keV were measured for different parameter settings of the analog channels. The baseline holder stage was identified as the responsible for the bandwidth limitation. For optimal configuration, no change in transfer function was observed and energy resolution degradation of 10-15 % was measured. Further tests will be performed on the next production batch to confirm the results with more channel statistics and to study the behavior for rate of 30000 cts/s/cm².

4.4 ASIC performance in radiation environment

Radiation hardness of IDeFX-HD circuit was evaluated during irradiation campaign on some ASIC test vehicles. Thanks to its hardened library of digital cells, no latch up was recorded at the Heavy Ions Facility of Louvain-la-Neuve (Belgium) up to a linear transfer energy (LET) of $135 \text{ MeV.cm}^2.\text{mg}^{-1}$. During this campaign, single event upsets were also studied. Registers are duplicated in the chip and permanently compared, and a SEU flag is sent out of the chip (and out of Caliste-SO after hybridization) in case of mismatch. The preliminary conclusion is that LET threshold for SEU is around $10 \text{ MeV.cm}^2.\text{mg}^{-1}$, in a similar way as for IDeF-X ECLAIRS that has some digital blocks in common [3]. From data about Solar Orbiter radiation environment and experimental data with IDeF-X ECLAIRS, we estimated the upset rate below 0.5 per ASIC for 10 year mission. In any case, the criticality of one event upset in Caliste-SO is low for the system (power, performance). The effect of total ionizing dose was also evaluated with a ^{60}Co gamma-ray source. Noise performance evolution is summed in Figure 11. The circuit is functional with no power consumption variation up to 200 krad and no performance degradation is visible before 40 krad. In assessment study, a sector analysis on STIX was performed and estimated the total dose to 20-30 krad at the ASIC level. Formal qualification with ASIC samples from the flight batch will be performed to confirm the results.

Figure 11: Noise characteristics of IDeF-X HD ASIC during the total ionizing dose test campaign measured on one channel with no input capacitance and a leakage current imposed between 20 and 50 pA.

5. CONCLUSION

Caliste-SO CdTe hybrid detectors were designed and fabricated to answer to the specifications of small hard X-ray spectrometer units to be placed behind each collimator of the STIX instrument. Spectral and timing capabilities have been demonstrated on the first samples. They will be integrated in 2014 in the engineering model of STIX to validate the full acquisition chain of the instrument. Designs and processes to fabricate the CdTe pixel sensors and the Caliste bodies were both improved during the implementation phase to produce flight quality devices. Meanwhile test set-ups and procedures were validated. The next Caliste-SO batch is in production. Further characterizations will be lead on these samples to improve the knowledge on the devices, in high rate conditions and in proton environment in particular, before integrating them in the STIX qualification model in 2015.

REFERENCES

- [1] Müller, D., Marsden, R. G., St. Cyr, O. C., Gilbert, H. R., “Solar Orbiter – Exploring the Sun-heliosphere connection”, *Solar Physics* 285, 25-70 (2013).
- [2] Benz, A. O. et al., “The Spectrometer Telescope for Imaging X-ray (STIX) on board the Solar Orbiter mission”, *Proc. SPIE* 8443, paper 8443-131 (2012).
- [3] Lin, R. P. et al., “The Reuven Ramaty High Energy Solar Spectroscopic Imager (RHESSI)”, *Solar Physics* 210, 3-32 (2002).
- [4] Gevin, O. et al., “IDeF-X ECLAIRS: a CMOS ASIC for the Readout of CdTe and CdZnTe Detectors for High Resolution Spectroscopy”, *IEEE Transactions on Nuclear Science* 56, 2351-2359 (2009).