Nuclear Inst. and Methods in Physics Research, A 953 (2020) 163176

Contents lists available at ScienceDirect

Nuclear Inst. and Methods in Physics Research, A

journal homepage: www.elsevier.com/locate/nima

Edgeless silicon sensors fabricated without support wafer

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ARTICLE INFO

Keywords:
Silicon radiation detectors
X-ray detectors
Particle tracking detectors
Edgeless sensor
Active edge

ABSTRACT

Silicon radiation detectors with minimum dead area in the sensor periphery are desirable and sometimes necessary for many applications in nuclear medicine, high energy physics, and X-ray science. The dead area typically includes a guard ring structure that is required for facilitating a uniform electric field distribution around the active area of the sensor, and consequently assuring high breakdown voltages, as well as for limiting the active area leakage current. The dead sensor periphery can be drastically reduced or even completely eliminated by replacing the conventional guard ring structure with the so-called "active-edge". The active edge is fabricated by etching through-substrate trenches surrounding the active area of the sensor using a micromachining technique known as deep reactive ion etching, followed by passivation of trench walls with doping. The active edge thus provides an excellent isolation of the active area from defects resulting from sensor separation while occupying only negligible physical space. Several laboratories worldwide have investigated the fabrication of active-edge sensors using a support wafer, which is required to provide mechanical integrity once the trenches are etched. However, the post-processing removal of the support wafer is a cumbersome and unreliable step, making this fabrication approach unsuitable for high yield manufacturing. We have recently developed a new fabrication method that eliminates the challenges associated with processing on a support wafer and thus facilitates mass-manufacturing. We have successfully demonstrated the fabrication of edgeless sensors with edge insensitivity of < 10 micrometer at SINTEF without the need for a support wafer. The design, fabrication, simulation and characterization results of these sensors are reported in this paper.

1. Introduction

Silicon radiation sensors typically possess an inactive region at the sensor periphery due to the presence of a termination structure consisting of the following elements, ordered from the innermost to outermost one:

(i) a grounded ring, known as Current-Collection Ring (CCR) or Current-Termination Ring (CTR) or Bias Ring (BR), for the reduction of leakage current flowing into the active area
(ii) multiple floating rings in most designs to ensure an even distribution of the electrostatic potential in the edge region, delivering higher breakdown voltages and better stability
(iii) additional space and structures between the active region and dicing lane of the sensor to shield the active area from the defects created by the dicing process.

This dead region of the sensor can be as wide as a few mm depending on the thickness and resistivity of the wafer, and operational requirements of the sensor [1–4].

There has been a growing need for "edgeless" silicon sensors, i.e. sensors with reduced or zero dead periphery, to reduce geometrical inefficiencies for applications in high energy physics, X-ray experiments at synchrotrons and Free Electron Lasers (FELs), and medical imaging. For example, the new pixel sensors for the High Luminosity LHC (HL-LHC) upgrade of the ATLAS pixel tracker must have significantly reduced insensitive area in order to achieve high geometrical acceptance without overlapping adjacent modules due to material budget restrictions and tight mechanical constraints [5–8]. In X-ray imaging using hybrid pixel detectors, the large detection area is obtained by tiling multiple detector modules into arrays; however, the dead periphery of individual modules causes a loss of information between the modules, resulting in seamed images. Seamless large area images can be captured by replacing conventional silicon sensors with edgeless sensors in a mosaic fashion in combination with a Through-Silicon-Via (TSV) technology applied to the readout chip [9–14]. For some X-ray imaging applications, silicon detectors are operated in edge-on configuration (incident beam is parallel to the surface of the detector) for a high X-ray absorption efficiency up to energies of ~100 keV [15].

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https://doi.org/10.1016/j.nima.2019.163176
Received 5 September 2019; Received in revised form 20 November 2019; Accepted 25 November 2019
Available online 27 November 2019

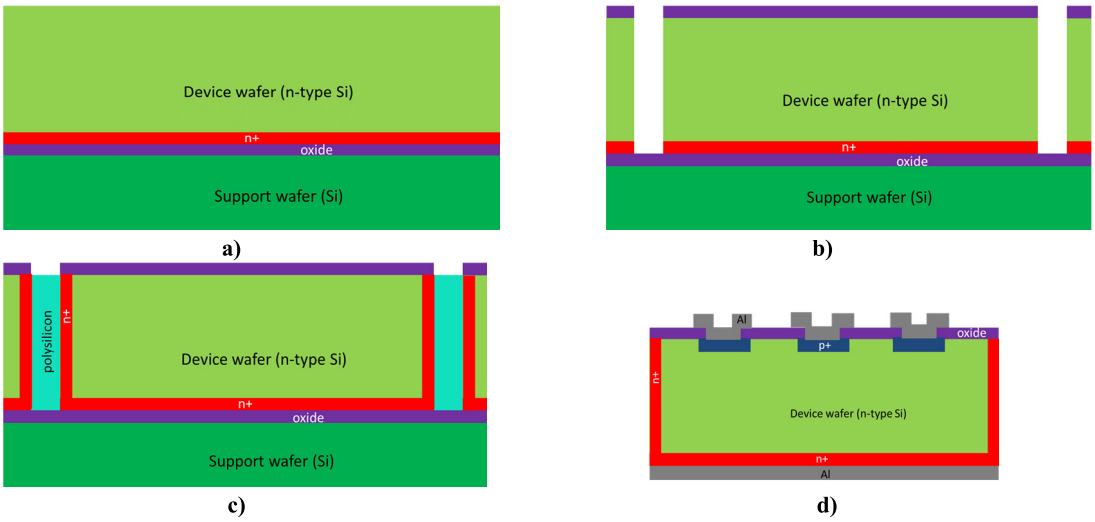


Fig. 1. Key processing steps involved in the fabrication of edgeless sensors by the traditional approach with a support wafer: (a) Fusion bonding of the sensor wafer to a support wafer after backside doping of the sensor wafer (b) DRIE of a continuous wafer-through trench around the active area of each sensor (c) Doping of the trenches, in some cases followed by polysilicon filling (d) Standard planar sensor processing and then removal of the support wafer and backside metallization.

However, the dead edge of silicon sensors forms a thick entrance window for X-rays, preventing the detection of X-rays with energy less than ~10 keV. With edgeless detectors, the sensitivity can be extended to energies below 5 keV and the detection efficiency can be improved significantly up to ~30 keV in the edge-on operation [16].

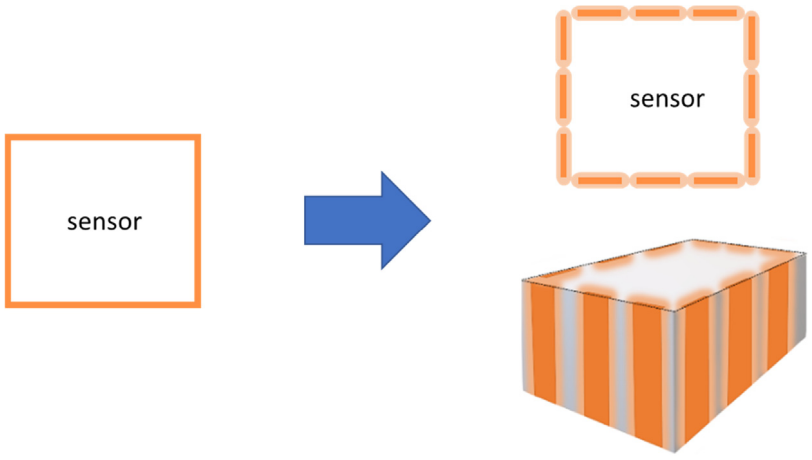
The "active edge" concept was first demonstrated in 2001, as an extension of 3D sensor technology [17], and the first full active-edge planar silicon sensors were fabricated in 2006 at Stanford Nanofabrication Facility [18,19]. Since then, several foundries including SINTEF (Norway), VTT (Finland, now its spin-off Advacam) and FBK (Italy) have investigated this technology with an aim in bringing it to a full manufacture level [5,6,13,16,20,21]. The active edge feature is realized by replacing the insensitive sensor periphery with a through-wafer trench surrounding the active area of the sensor and subsequently passivating the walls of the trench with doping. Any source of high leakage current due to the edge termination is thereby eliminated. The fabrication of edgeless sensors normally starts with direct bonding of the sensor wafer to a support wafer. This is needed to maintain the integrity of the wafer after the etching of trenches surrounding individual sensors so that the subsequent wafer-level processing steps can be carried out. After all wafer-level sensor processing is completed, the support wafer has to be removed for most applications, which has been proven to be extremely challenging. This has hindered the high yield manufacturability of edgeless sensors over many years, and therefore different fabrication approaches are necessary. We have recently developed a simplified and high throughput manufacture process at SINTEF for the fabrication of edgeless sensors with an edge insensitivity of <10 micrometer without using a support wafer. In this paper, we discuss the design, fabrication process, simulation and characterization results of our prototyping run.

2. Sensor design and fabrication

Fig. 1 shows the key fabrication steps of edgeless sensors based on the traditional approach requiring a support wafer [5,17–22]. First, the sensor wafer is bonded to a support wafer by direct (fusion) bonding. Next, a continuous through-wafer trench is opened by Deep Reactive Ion Etching (DRIE) all around the active area of each sensor. The walls of the trenches are then heavily doped using the same dopant species as the backside to shield the sensor from DRIE-induced crystal defects located at the edge and thus prevent a high sensor leakage current. In some cases, the trenches are filled with polysilicon deposited by Low Pressure Chemical Vapor Deposition (LPCVD) for re-planarization of the wafer so that the subsequent photolithographic steps same as for the standard planar sensors can be carried out smoothly; for example, surface doping, contact hole opening, metallization and passivation. Finally, the support wafer is removed by a back-grinding and/or etching (either plasma or wet chemical etching) process, and the sensors are singulated. The removal of the support wafer is a difficult and often a risky and damaging process, making this traditional approach far from being ideal for mass production with high yield and moderate cost.

We have recently pursued a new approach to fabricate edgeless sensors, which does not require a support wafer and therefore eliminates the processing redundancies and complexities associated with bonding and removal of the support wafer. This so-called "Perforated Edge" approach was first proposed in 2012 [23] but we are first to demonstrate this approach experimentally. The processing of edgeless sensors without a support wafer is realized by a segmented (or perforated) trench design instead of a continuous trench as depicted in Fig. 2. In this approach, the mechanical integrity of the sensor wafer is ensured by the silicon left in place between the trench segments. After gas-phase doping of the trench segments, the doping of the unetched region between segments is performed by deep drive-in of the dopants, effectively forming a fully doped periphery. Once the wafer processing is completed, the edgeless sensors can be singulated by conventional saw dicing.

We have fabricated a batch of edgeless sensors on 300 μm thick, 6-inch, n-type silicon wafers with resistivity of 6 000–12 000 Ω cm with the "Perforated Edge" approach. The wafer layout consists of pad diodes, micro-strip sensors and Medipix/Timepix compatible pixel sensors [24] with segmented active-edge trench design. Fig. 3 shows the picture of a completed wafer and close-up pictures of a pad diode and pixel sensor on the wafer. A scanning electron microscope (SEM) image of the cross section of a trench segment is also shown in the same figure. The aspect ratio (ratio of width to depth) of the through-substrate trench is ~1:50. The edgeless pad diodes are particularly useful for a quick verification of the fabrication approach by (*i*) measurement of the active area leakage current at wafer level and assessment of die yield, and (*ii*) monitoring how the leakage current changes after dicing at various distances from the segmented trench to determine the minimum insensitive area achievable, in the same way as the "Slim Edge" approach [25].



a) Continuous active-edge trench design (top-view)

b) Perforated active-edge trench design (top-view at the top and 3D view at the bottom)

Fig. 2. Illustration of active-edge fabrication without using a support wafer. The continuous active edge trench surrounding the active area of sensor (a) is replaced with segmented or perforated trenches (b). The unetched silicon between trench segments, which holds the wafer intact after DRIE, is doped by deep drive-in of trench dopants, resulting in a fully doped edge.

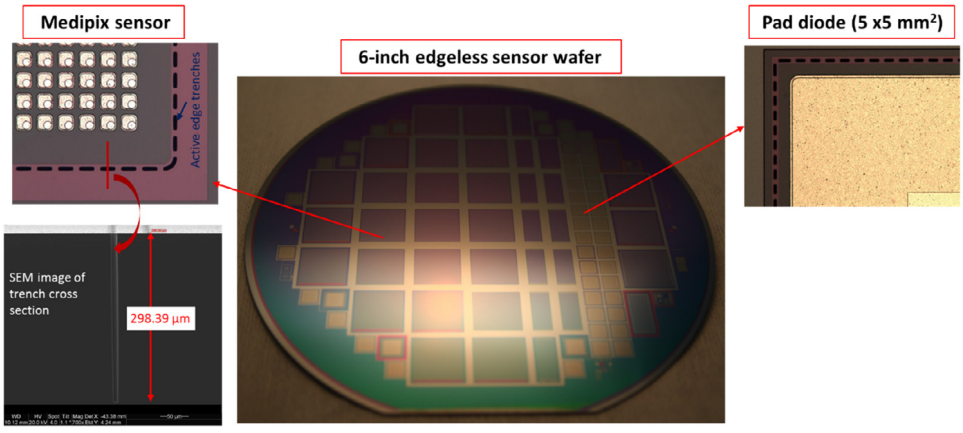


Fig. 3. Pictures of a completed 6-inch wafer including edgeless pad, strip and pixel sensors with segmented active edge trench design and a cross sectional SEM image showing that the trench is going through the entire wafer thickness (aspect ratio: ~1:50).

3. Sensor simulation and characterization

3.1. Electrical simulation and characterization

A numerical model of a pad diode with perforated edge was created using the SYNOPSYS Sentaurus TCAD tools [26]. The aim of the simulation was to demonstrate how the incremental diffusion depth of the trench doping can deliver a perfect isolation from the dicing lane such that the sensor performance in detection of incoming radiation remains the same as if guard rings were present. The numerical model used for electrical simulations is shown in Fig. 4a. This structure replicates a portion of the edge termination of the fabricated pad diode shown in Fig. 3. The dimensions of the structure are $250 \times 85 \times 300$ µm^3, which were carefully chosen in order to minimize the total number of nodes in the numerical mesh while still producing a reliable simulation structure. The edge termination is composed of multiple n+ trench segments separated by 20 µm of silicon. The distance from p+ pad to the trench segments was designed to be 50 µm for the fabricated diode so the same distance is used in the simulation. The dicing region outside the segmented trench is modeled as a volume in which the generation/recombination carrier lifetimes are reduced to 1 ns to simulate the damage caused by diamond saw [25]. The avalanche models are disabled, in order to account only for the effect of the damaged dicing volume. The device is biased using a positive bias ramp applied to the uniform n+ implantation on the back, which is also electrically connected to the n+ trenches, with respect to the grounded p+ pad implant. The doping of the trenches is modeled using an error function, where the doping remains constant at 1×10^{20} cm^{-3} up to the inflection point at a depth of 1 µm. The depth of the doping profile is given as the point where the error function reaches the value of the bulk doping (5×10^{11} cm^{-3}).

The I–V simulation was carried out for different dopant drive-in depths increasing in steps of 1 µm. The simulated I–V curves are reported in Fig. 4b. After reaching full depletion, the depletion region continues to laterally expand toward the edge. For shorter dopant diffusion depths, a sharp increase in current can be observed above a bias voltage of 100 V. This indicates that the trenches are not yet able to prevent the depletion region from reaching the dicing region. As the doping of the trenches becomes deeper, a true active-edge like structure is formed, completely shielding the sensor's active volume from the

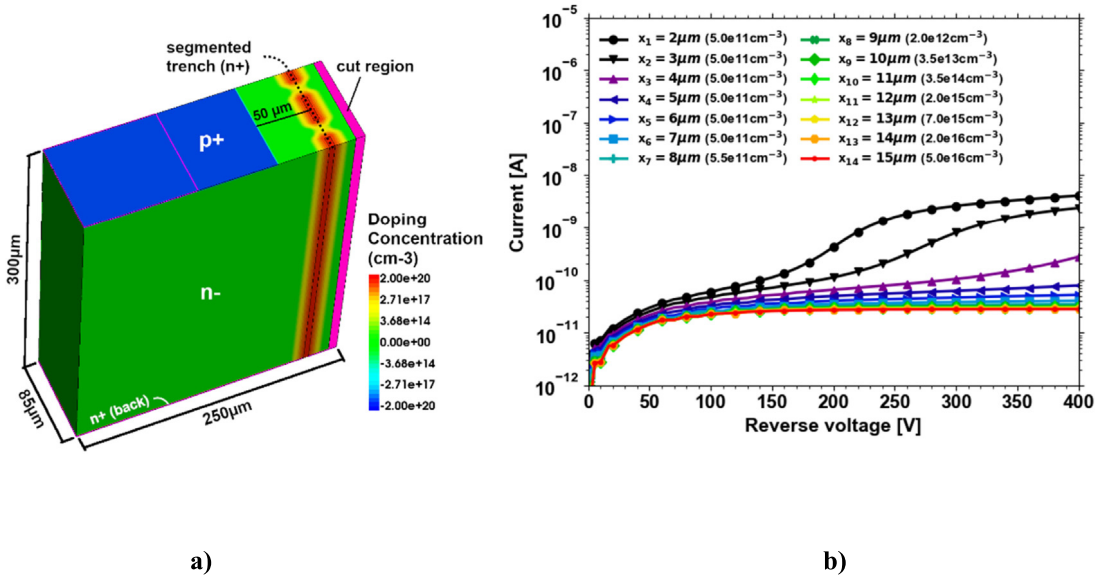


Fig. 4. Simulation of pad diode with perforated edge (a) diode structure (b) corresponding I–V characteristics for different dopant drive-in depths. The doping concentration in the middle of the silicon region between two trenches is reported inside the parentheses in the legend of (b).

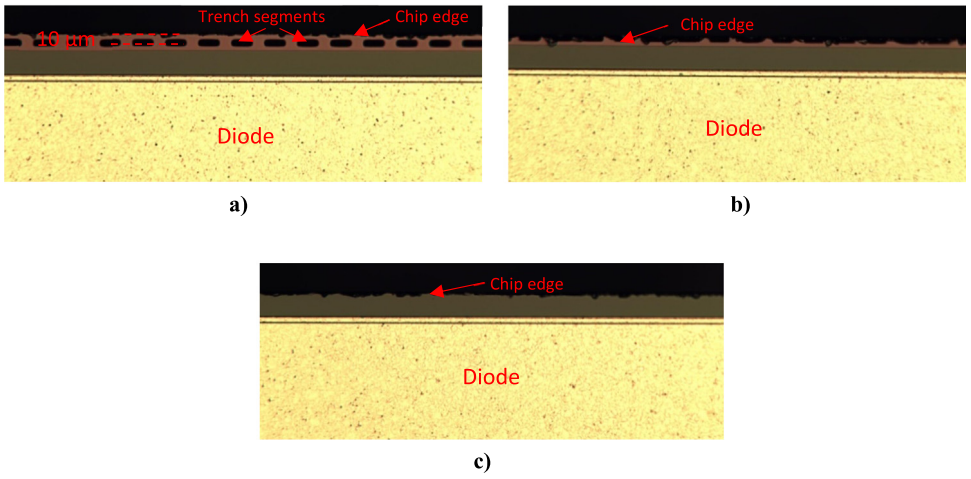


Fig. 5. Edgeless diode (top view) diced (a) 10 μm outward from the center of segmented trench (*center*+10 μm) (b) through the center of segmented trench (*center*) (c) 10 μm inward from the center of segmented trench (*center*-10 μm).

dicing region, and thereby preventing an early increase in reverse current. It is important to observe that the shielding of the active-area from the dicing region starts to become effective even before the doping of neighboring trenches reach each other (Fig. 4b, curves x_1 to x_6). The increased proximity of the doping profiles provides a preliminary electrical shielding which allows less current to be injected from the dicing region. This effect was previously observed in [27] for similar structures where the doping of neighboring trenches were not joined. The successful formation of a doped trench requires the doping of the trenches to diffuse for at least 10 μm into the silicon bulk, so that the doping concentration in between two trenches increases by at least 2 orders of magnitude (curve x_9 in Fig. 4b).

After proof-of-concept demonstration with numerical simulations, electrical measurements were performed on our 5 mm × 5 mm edgeless diodes fabricated by the Perforated Edge approach. The depletion voltage extracted from Capacitance–Voltage (C–V) measurements is ~50 V. Fig. 5 shows pictures of edgeless diodes diced with diamond saw at various distances from active-edge trenches. Fig. 6 shows the measured diode leakage current as a function of reverse bias voltage for different dicing distances with respect to the center of trench segments, together with the simulated one before dicing. Avalanche models were included in the I–V simulation this time in order to estimate breakdown voltage of the diode. The measurement and simulation results show a very good agreement. The leakage current of the diodes at full depletion voltage is <100 pA, which is very similar to the leakage current of their counterparts with conventional guard-ring structure. The breakdown voltage is still above 300 V even after dicing through the center of the trench segments. After dicing 10 μm inwards from the center of trench segments (as shown in Fig. 5c), the leakage current starts to dramatically increase at 135 V as the depletion region starts to reach the cracks at the physical edge of the sensor formed by dicing. Nevertheless, this increase occurs still above the full depletion voltage. As can be seen in Fig. 5, the saw dicing creates chipping and cracks in order ~5 μm, which limits the minimum dead periphery achievable

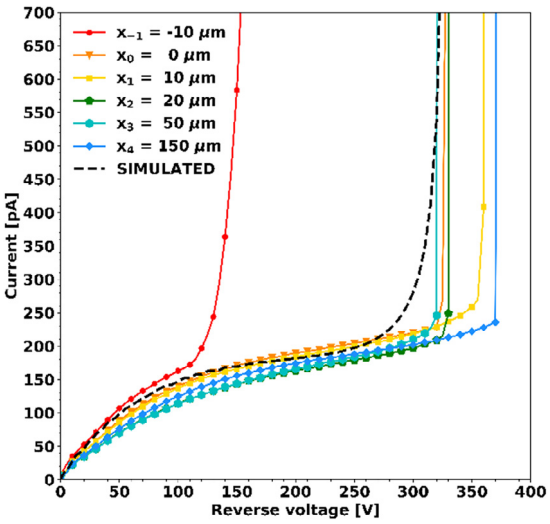


Fig. 6. The measured I–V characteristics of edgeless diodes diced at different distances from the center of segmented trenches, together with the simulated one before dicing.

with the Perforated Edge approach to this extent. Theoretically, one can dice inwards from the trenches, very close to the end of the diffusion region of trench dopants without causing an early increase in leakage current. With smoother dicing methods such as laser dicing which results in less significant edge chipping, the dead periphery can possibly be reduced even further.

In order to understand the charge collection behavior of edgeless sensors, the electrostatic potential distribution was also simulated. The numerical model used for this study was a strip detector with strip pitch of 75 μm and strip width of 20 μm. The simulated structure includes the first nine strips from the edge. The distance between the outermost strip and the trench termination is set to 125 μm. This was to replicate the fabricated edgeless strip detector, whose charge collection performance is studied thoroughly in Section 3.2. Fig. 7 shows the simulated electrostatic potential distribution and drift lines near the edge of the sensor at bias voltages of 60 V and 120 V. Note that since the simulation was done in 2D, the electrostatic potential distribution presented here is valid for the region reasonably away from the tips of the strips. The strip sensor is still not fully depleted at 60 V as seen in Fig. 7a whereas the fabricated diode had a depletion voltage of ~50 V. This should not come as a surprise since the strip detector with a strip width/pitch ratio of 20/75 would require more voltage than a pad diode to fully deplete due to lateral depletion. The outermost strips have rather distorted drift lines, which will result in a non-uniform charge collection near the active edge. For example, if a particle passes through the detector in the area between the first (outermost) strip and the edge, the charge generated in the top part of the sensor will be collected by the first strip, while the charge generated in the bottom of the detector will be collected by the second strip (following the field lines). In addition, this brings potential issues similar to charge sharing, because if the same signal is shared between multiple strips, it may not go over the threshold. Comparing the field lines in Fig. 7a and b, it is evident that the second strip should collect more charge at 120 V than at 60 V with respect to the first strip since the field lines pointing to the second strip occupy more volume at 120 V. This has also been observed experimentally as discussed in Section 3.2. The non-uniform charge collection due to the E-field bending near the sensor edge can be corrected by modifying the applied bias and/or by applying a software correction during the data post processing.

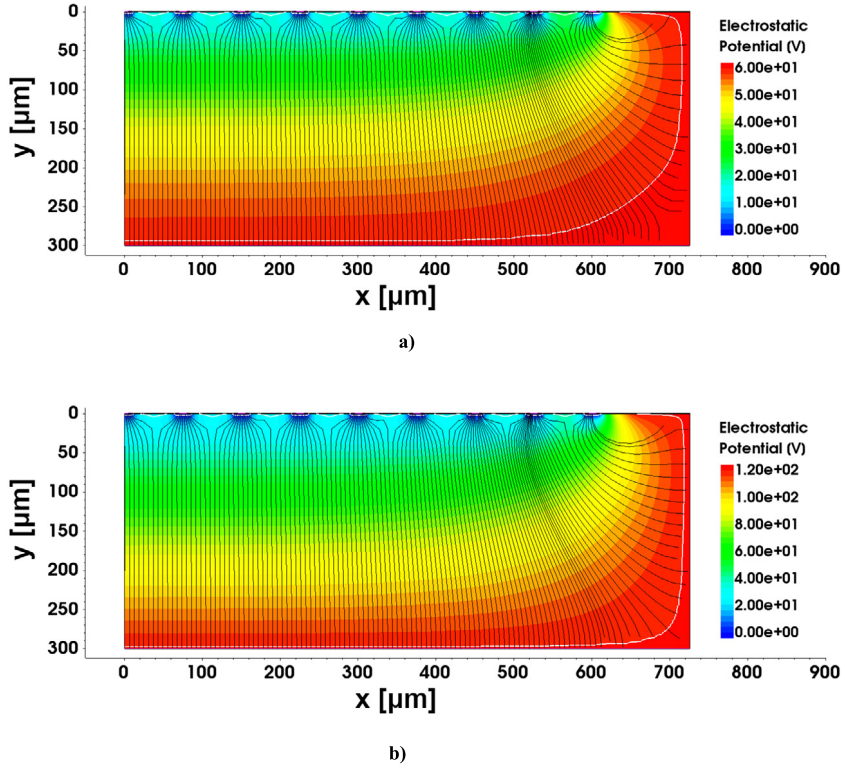


Fig. 7. 2D simulation of electrostatic distribution and electric field lines in edgeless strip detector near the edge strips (a) at reverse bias of 60 V, (b) at a reverse bias of 120 V. The white lines show the boundary of the depletion region.

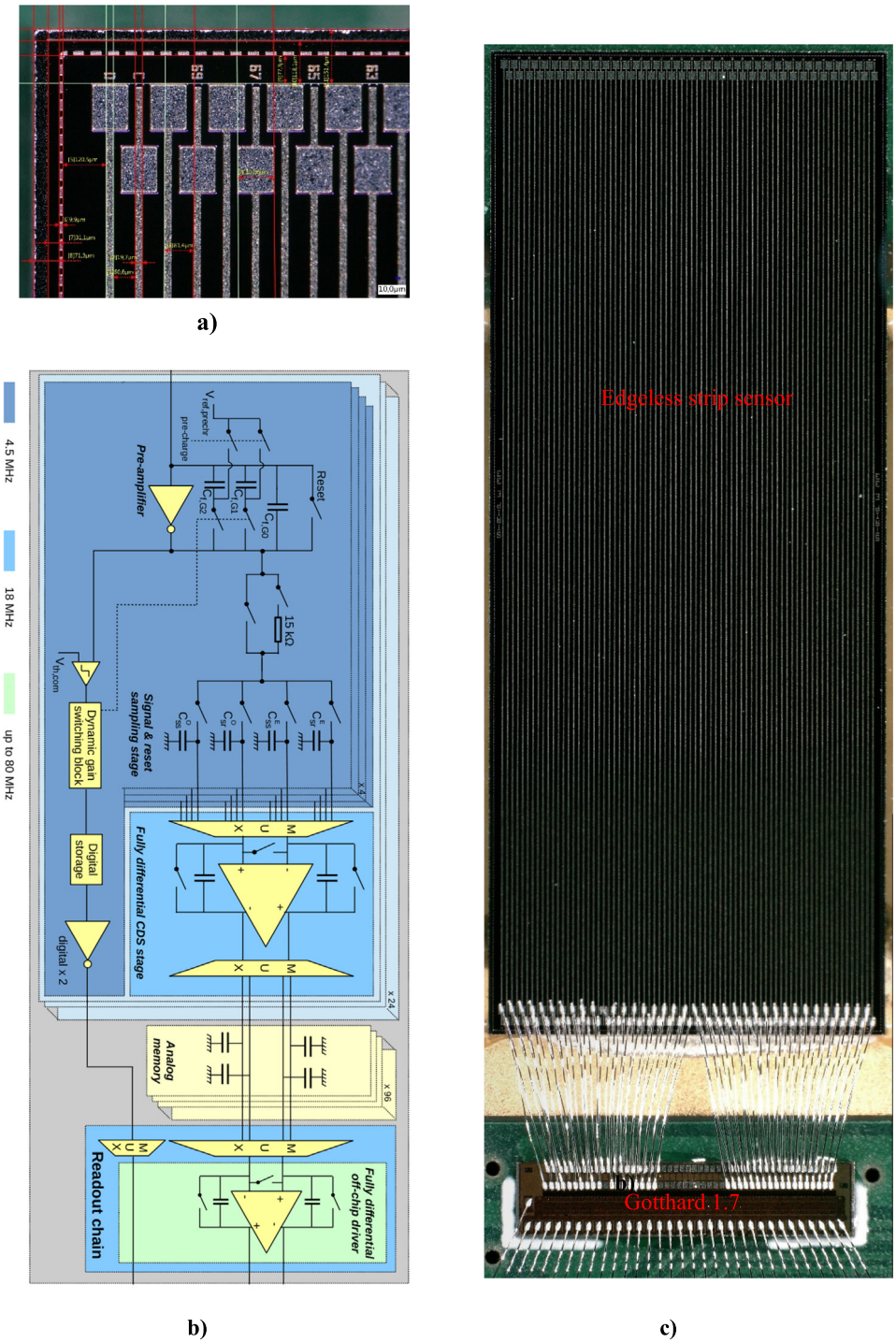


Fig. 8. (a) Microscope image of edgeless strip sensor corner (b) Gotthard-1.7 readout chip schematic (c) Edgeless strip sensor wirebonded to the Gotthard 1.7 readout chip.

3.2. Functional characterization

Two randomly picked edgeless micro-strip sensors were wire-bonded to Gotthard 1.7 [28], a charge-integrating readout chip (ROC), for functional testing of the sensors (Fig. 8). The sensor consists of 74 strips with a pitch of 75 μm, and a length of 14.34 mm. The sensors were diced at a distance of 50 μm from the trenches, leaving a frame as a safety measure for any damage that can happen during post-processing handling. As demonstrated in Section 3.1, without such a frame, the sensors electrically behave the same, and therefore there is no need to keep such frame once a handling protocol has been established.

The conversion gain was determined from measurements with florescent X-rays from Cu target (K_α energy = 8.05 keV). The positions of photon peaks in the Analog–Digital Unit (ADU) histogram were extracted from a Gaussian fit to each individual peak. The extracted peak position in terms of ADU was plotted as function of energy which is given by the energy of the K_α X-ray florescence times the number of photons. The conversion gain (*gain [ADU]*) is then obtained from the

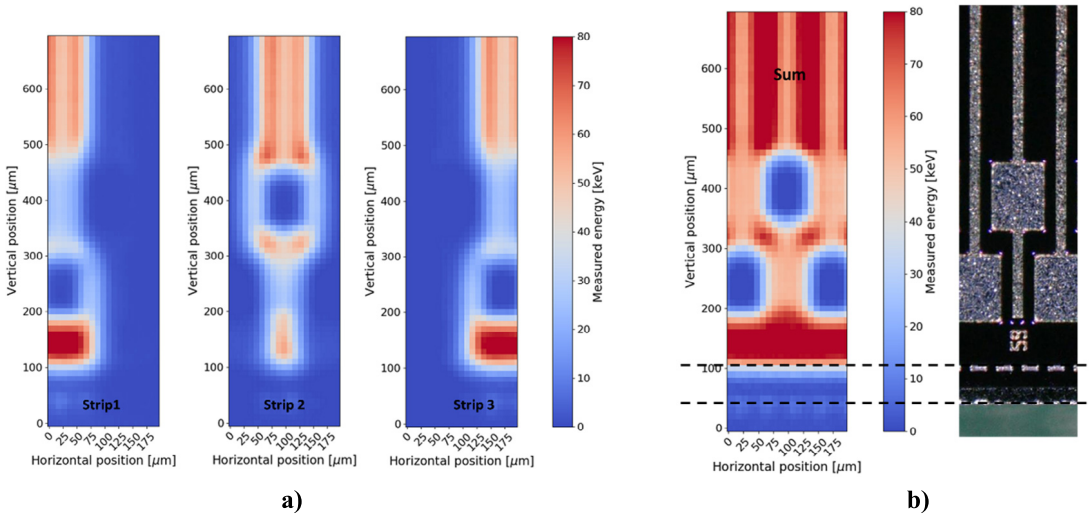


Fig. 9. Laser scan results of three strips in the center of an edgeless sensor at a bias voltage of 60 V: (a) collected charge as a function of laser position for each individual strip, (b) sum of the charge collected by all three strips in this scan. Figure (a) and (b) share the same color scale. The two dashed horizontal lines in (b) show the positions of the trench segments and the physical edge of the sensor.

Table 1
Hamamatsu strip detector with guard rings vs. SINTEF edgeless strip detectors. C_{dep}: capacitance of individual strips to the backside; C_{int}: interstrip capacitance between two neighboring strips.

	Hamamatsu sensor with guard rings ring termination	SINTEF edgeless sensor *A*	SINTEF edgeless sensor *B*
Pitch	50 μm	75 μm	
Thickness	320 μm	300 μm	
Length	8 mm	14.34 mm	
C_{dep}	131.6 fF	402.7 fF	
C_{int}	614 fF	1160 fF	
Gain	25.2 ADU/keV	23.5 ADU/keV	
Leakage/strip	0.12 nA/strip	0.22 nA/strip	0.18 nA/strip
Leakage/area	30 nA/cm^2	19.1 nA/cm^2	15.7 nA/cm^2
Noise @ 5 μs	300 e$^-$	400 e$^-$	

slope of a linear fit to this plot. The integrated leakage current was measured in a light–tight box for 5 μs multiple times and a Gaussian fit was made to the histogram of ADU values to extract the standard deviation, $\sigma[ADU]$. The noise was then obtained by $(\sigma[ADU]/gain[ADU/\text{keV}])$ x (1000/3.6 [eV]), where 3.6 [eV] is the mean energy required to create one electron–hole pair in silicon by ionizing radiation. The methods used to determine the conversion gain, noise as well as leakage current have been described in detail in [29].

Table 1 shows the measurement results of our edgeless strip detectors in comparison with a commercial strip detector from Hamamatsu with conventional guard ring edge termination, which has been reported in [28,29]. The functional performance of the two types of sensors are very similar. The leakage current per strip is slightly higher for the edgeless sensors. However, when the leakage current is normalized to the sensor area, the edgeless strip sensors exhibit lower leakage current. The edgeless sensors in the investigations show higher capacitance mainly due to larger strip dimensions. This leads to slightly higher noise compared to the commercial sensor with guard rings. The detector assemblies with edgeless sensors show comparable performance to the one with conventional sensor, and no major impact due to the implementation of the segmented active-edge trenches, for example the increase of leakage current, was observed.

A laser scan was performed on the edgeless sensors with an infrared laser (wavelength of 1030 nm) to investigate uniformity of charge collection across the sensor. The measurements were carried out at bias voltage of 60 V, which is about the full depletion voltage, with the infrared laser entering from the strip side. Fig. 9 shows the measured charge (in keV after a pedestal correction and gain correction to the detector raw output), integrated over 5 μs, as a function of scan position of the laser for three adjacent strips in the center of the sensor. Fig. 9a shows the scan results for each individual strip while Fig. 9b shows the sum of output charge from all these three strips in this scan. The blue region in Fig. 9b indicates less collected charge which is mainly due to the absorption and reflection of the laser light by the aluminum layer on the strip side. The results clearly demonstrate that the response of individual strips in the center of the sensor are identical. Moreover, full efficiency (complete charge collection) is observed up to the vicinity of active-edge trenches (Fig. 9b). The lower efficiency in the vicinity of trenches is due to the lateral diffusion of trench dopants.

In addition, the laser scan was carried out on nine strips closest to the edge of the sensor in the corner region. Fig. 10a shows the charge collection as a function of laser position for each individual strip while Fig. 10b shows the superimposition of output charge from all these nine strips in this scan. The inner three of nine edge strips exhibit more or less uniform (or symmetric) charge collection as a function of laser position. Unlike the inner strips, non-uniform charge collection is observed for the outer strips as seen in Fig. 10a. In other words, more charge is collected when the laser is incident on the left side of the strip compared to when incident on the right side of the strip for outermost strips. This asymmetry becomes more and more prominent towards the sensor edge. This can be explained by the electric field bending at the edge of edgeless detectors which was discussed in Section 3.1.

A 1D laser scan was performed on the strips closest to the edge but around the center of the strips in the direction perpendicular to the length of the strips at different bias voltages to investigate the effect of electric field bending as a function of bias voltage. Figs. 11 and 12 show the results at bias voltages of 60 V and 120 V, respectively. The response was corrected for laser reflection and absorption by the metal on the strips by normalizing to the maximal summed charge when laser shots in-between strips where the reflection and absorption by the metal can be neglected. It should be noted that the lower maximum charge at 120 V is due to using a lower laser intensity compared to the operation at 60 V. As seen in Figs. 11c and 12c, the outermost strips collect more charge than the inner strips due the electric field bending, and the charge collected by the outermost strips is strongly

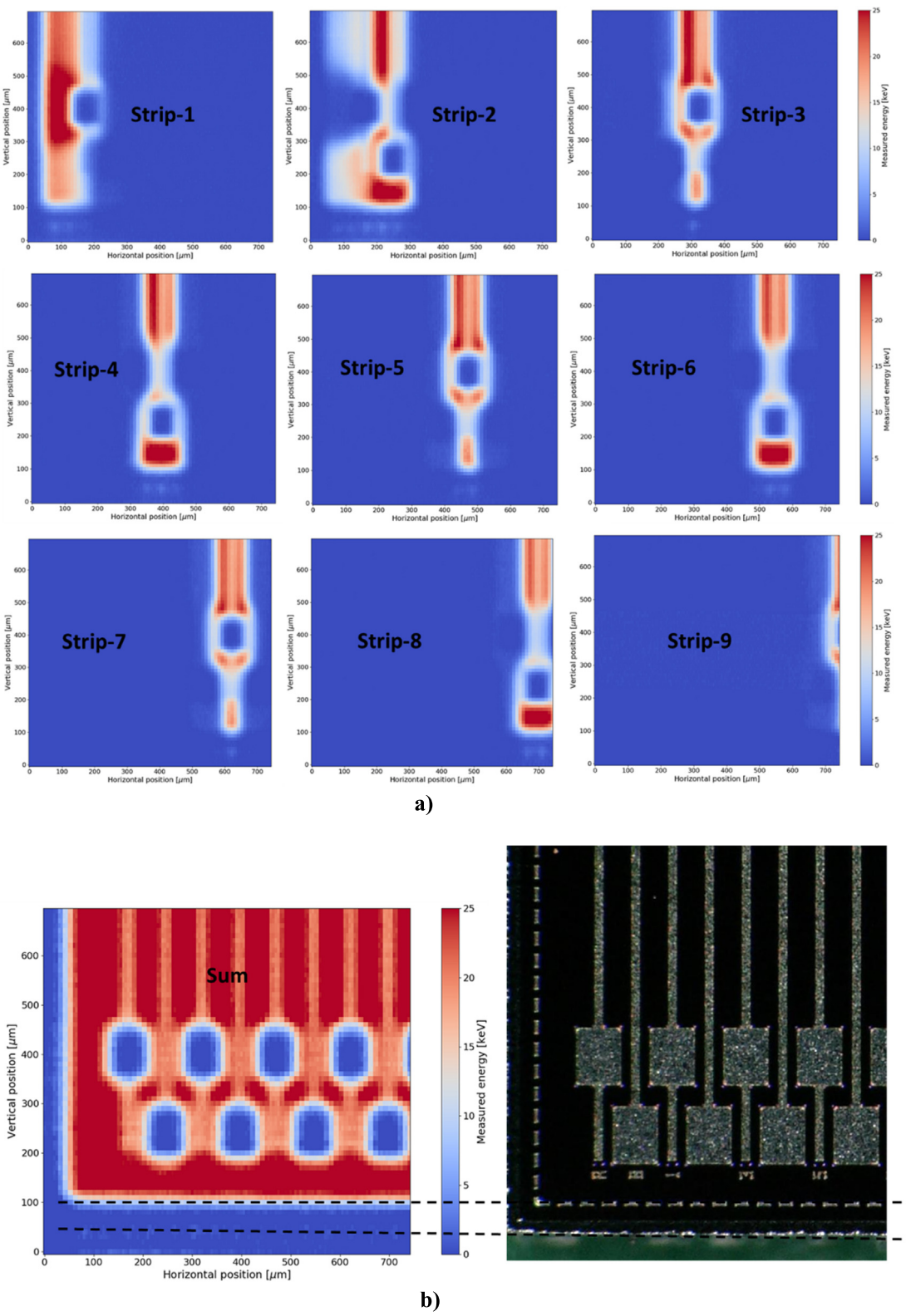


Fig. 10. Laser scan results of nine outermost strips of an edgeless sensor at a bias voltage of 60 V: (a) collected charge as a function of laser position for each individual strip, (b) sum of the charge collected by all nine strips in this scan. Figure (a) and (b) share the same color scale. The two dashed horizontal lines in (b) show the positions of the trench segments and the physical edge of the sensor.

dependent on the applied bias voltage which modifies the electric field distribution. The higher ratio of charge collection by strip-2 to strip-1 at 120 V compared to 60 V is consistent with the simulated potential distribution in Fig. 7. The non-uniform charge collection by edge strips/pixels has been extensively investigated before and a simulation model has been developed to predict the charge collection

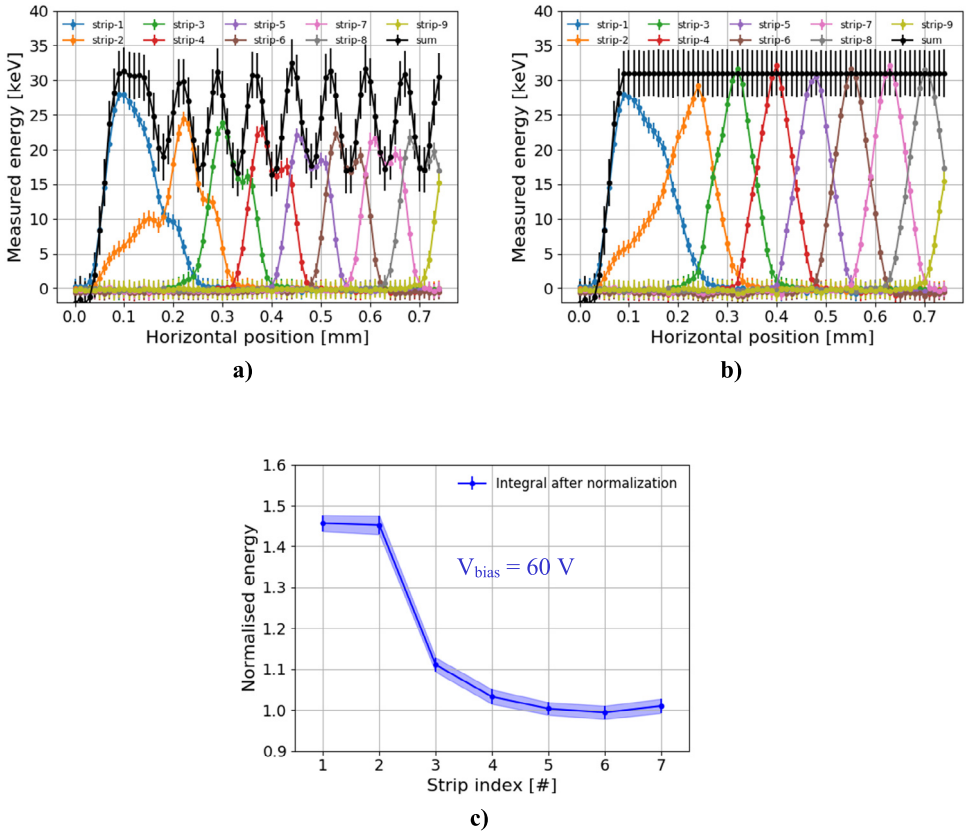


Fig. 11. Results of 1D laser scan around the center of nine edge strips in the direction perpendicular to the length of the strips at bias voltage of 60 V (a) Collected charge as a function of laser position for each strip and sum of all nine strips (b) Collected charge as a function of laser position for each strip and sum of all nine strips after correction for reflection of the laser light from the metal on the strips. The position in the horizontal axis refers to the absolute position of the motor stage which carries the mounting mechanic and the detector during the scan. The position at 0.06 mm in the plot, giving half of the measured total charge, can be considered as the position in which the laser starts to shoot at the physical edge of the sensor. (c) Normalized charge integral (obtained by integrating the charge of individual strips in the preceding plot) vs. strip index.

behavior of edgeless sensors [6,10,30–32]. This effect can be corrected by a careful calibration based on the energy of X-ray photons and the operating condition.

4. Conclusion and outlook

We have successfully demonstrated the fabrication of 300 μm thick edgeless silicon sensors by the so-called "Perforated Edge" approach without using a support wafer. The insensitive sensor periphery can be reduced down to <10 μm with this approach. The edgeless sensors fabricated by this method show very similar electrical and functional performance compared to commercially available sensors with conventional guard-ring design. The charge collection by the edge strips of edgeless sensors shows some non-uniformity and dependence on bias voltage due to the electric field bending at the sensor edge as reported previously. Even though the investigations are done for edgeless strip sensors in this work, similar results and conclusions for the edgeless pixel sensors can be expected and drawn. This new fabrication method is simpler, more cost effective, and mass manufacturable compared to the traditional edgeless sensor fabrication methods that have been employed so far. Based on electrical measurement results of edgeless diodes at wafer level, the production yield is estimated to be similar to production yield of standard planar sensors with conventional guard-ring design.

Our approach can also be used for fabricating thicker edgeless sensors. However, for thicker wafers, the trench segments have to be designed wider in order to be able to etch deeper trenches (due to the aspect ratio limitation of DRIE). This implies that more polysilicon depositions will be needed to fill the trenches and additional etching will be required to remove the thicker polysilicon deposited on the wafer surfaces. Because of this reason, we expect our approach to practically work well up to wafer thicknesses of ~500 μm. The demonstration of the feasibility of our approach on 500 μm thick wafers is ongoing.

Fabrication of edgeless sensors thinner than ~300 μm faces the same challenges as the fabrication of traditional planar sensors with guard rings due to the unavailability of 6-inch wafers with such thicknesses (as they would not be mechanically robust enough to survive processing). Therefore, thinner planar sensors are typically processed on a support wafer (i.e., SOI or Si–Si wafers are used). For applications that do not allow a support wafer, different methods can be used. For example, a thick wafer can be thinned down selectively with a mask only under individual sensor areas, leaving thick supporting ribs between the sensors to keep the wafer intact during processing. After the wafer processing is completed, the thin sensors are separated from the supporting ribs through dicing. This method can be used to fabricate sensors down to thicknesses of ~50 μm. By combining this method with the "Perforated Edge" approach, thin edgeless sensors without support substrate can be manufactured.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

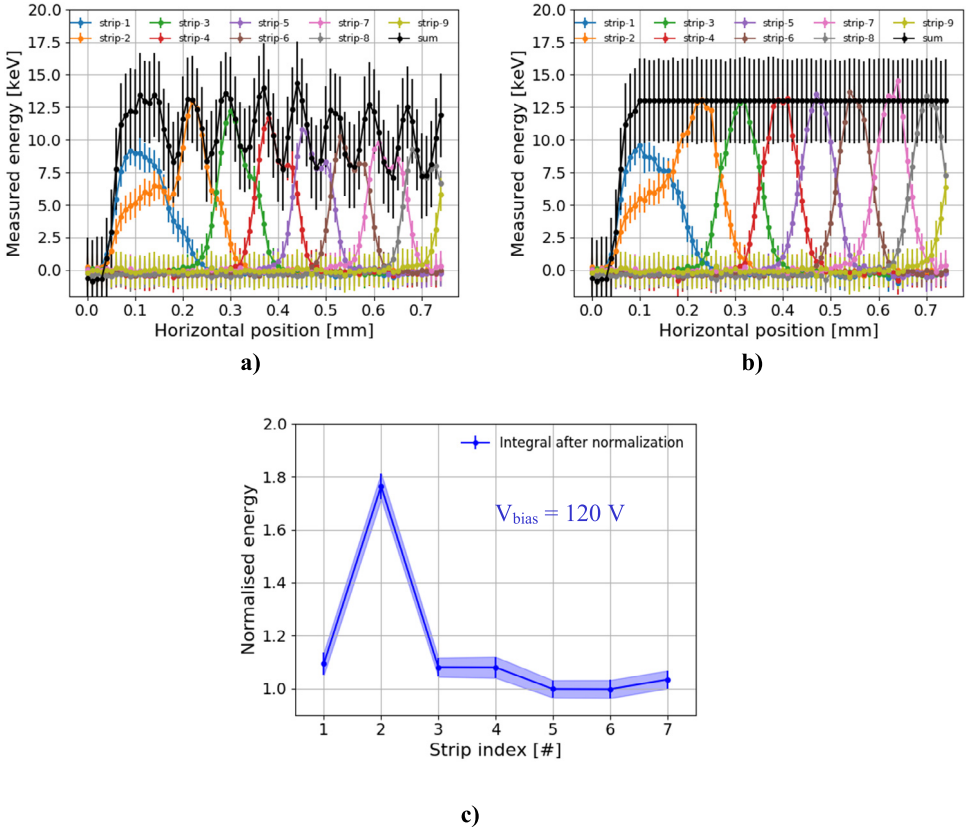


Fig. 12. Results of 1D laser scan around the center of nine edge strips in the direction perpendicular to the length of the strips at bias voltage of 120 V (a) Collected charge as a function of laser position for each strip and sum of all nine strips (b) Collected charge as a function of laser position for each strip and sum of all nine strips after correction for reflection of the laser light from metal on the strips (c) Normalized charge integral (obtained by integrating the charge of individual strips in the preceding plot) vs. strip index.

CRediT authorship contribution statement

Ozhan Koybasi: Conceptualization, Methodology, Validation, Investigation, Writing - original draft, Writing - review & editing, Visualization, Project administration. **Jiaguo Zhang:** Validation, Formal analysis, Investigation, Writing - review & editing, Visualization. **Angela Kok:** Conceptualization, Methodology, Writing - review & editing, Project administration. **Anand Summanwar:** Investigation. **Marco Povoli:** Methodology, Writing - review & editing, Visualization. **Lars Breivik:** Conceptualization, Methodology. **Anna Bergamaschi:** Supervision. **Bernd Schmitt:** Supervision.

Acknowledgments

The authors would like to thank Leny Nazareno and other process engineers/operators at SINTEF MiNaLab for their contribution on wafer processing; and Nicolas Lietaer, Erik Poppe, Sigurd Moe and Trond Hansen from SINTEF for the useful discussions and support on sensor fabrication.

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