Published by IOP Publishing for Sissa Medialab

Received: *October 21, 2022*
Accepted: *December 12, 2022*
Published: *January 17, 2023*

Topical Workshop on Electronics for Particle Physics
Bergen, Norway
19–23 September 2022

Characterisation of the first digital modules with RD53B-CMS readout chips for the Phase-2 Upgrade of the CMS Inner Tracker

M. Missiroli on behalf of the CMS Collaboration

Paul Scherrer Institut, Forschungsstrasse 111, 5232 Villigen, Switzerland
Physik-Institut, Universität Zürich, Winterthurerstrasse 190, 8057 Zürich, Switzerland

E-mail: marino.missiroli@psi.ch

Abstract: To cope with the challenges posed by the High-Luminosity LHC, the CMS experiment will feature a new silicon tracker. The modules of the upgraded inner tracker are hybrid silicon pixel modules based on a new readout chip, developed by the RD53 collaboration. Compared to the readout chip of the current pixel detector, the RD53 chip is capable of sustaining higher hit rates and radiation levels, as well as enabling the use of serial-powering chains. The qualification of the latest version of this chip (RD53B) is underway, and it will lead to the final version of the readout chip to be used in the CMS inner tracker during the HL-LHC. First digital modules featuring the RD53B-CMS chip have been assembled in 2022 (the term digital module denotes a module assembly with readout chips, but without sensors bonded to them). This contribution presents results of tests on these first prototype modules.

Keywords: Particle tracking detectors (Solid-state detectors); Radiation-hard detectors

https://doi.org/10.1088/1748-0221/18/01/C01027

Contents

1 Introduction

During the next long shutdown of the Large Hadron Collider (LHC), set to start in 2026, the accelerator will be upgraded to reach an instantaneous luminosity of up to $7.5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ in the ultimate performance scenario (corresponding to up to 200 pileup collisions per bunch crossing), and deliver an integrated luminosity of up to $4000\,\mathrm{fb}^{-1}$. The Compact Muon Solenoid (CMS) experiment [1] will undergo a series of upgrades to maintain, and possibly improve, its physics performance throughout the HL-LHC. This includes the installation of a new and improved silicon tracker, referred to as the CMS Phase-2 tracker [2]. The innermost part of this system, the inner tracker, will be comprised of hybrid modules featuring pixel sensors bump-bonded to read-out chips (ROCs). The pixel sensors of the Phase-2 inner tracker are characterised by higher granularity ($25 \times 100\,\mu\mathrm{m}^2$ in pixel size) and reduced thickness ($150\,\mu\mathrm{m}$) compared to the current pixel detector. In addition, the Phase-2 inner tracker will extend the geometric acceptance of the current system, providing coverage for tracks with pseudo-rapidity up to $|\eta| = 4.0$. The upgraded tracker will be comprised of three sub-systems: the Tracker Barrel Pixel (TBPX), the Tracker Forward Pixel (TFPX), and Tracker Endcap Pixel (TEPX) subsystems. Figure 1 (left) shows the layout of one quarter of the Phase-2 inner tracker. Figure 1 (right) shows a technical drawing of one TEPX half-disc, including the pixel modules distributed across three of its rings. A complete description of the Phase-2 tracker system can be found in ref. [2].

The ROC, developed by the RD53 collaboration using 65 nm CMOS technology, is designed to cope with hit rates up to 3–4 $\mathrm{GHz/cm}^2$ for trigger latencies up to 12.5 µs and radiation levels up to 500 Mrad. It features shunt low-dropout (SLDO) regulators to enable the operation of multiple modules (up to 12) in serial-powering chains, a design choice aimed at minimising the material budget of the detector. It also provides the possibility of merging readout data from two or four chips on a module into a single readout lane: this functionality, referred to as "data merging", allows to minimise the number of readout links for modules exposed to lower rates of incident particles.

2023 JINST 18 C01027

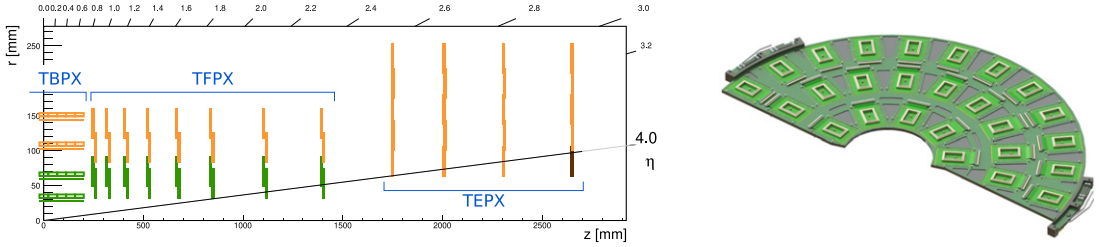

Figure 1. Left: layout of one quarter of the Phase-2 inner tracker in the *r*-*z* view (updated from ref. [2]). Right: technical drawing of one half-disc of the TEPX subsystem, showing pixel modules (light green) connected to the disc's printed-circuit board (dark green).

The first version of the RD53 readout chip (RD53A) [3] was a demonstrator chip, and it has been tested extensively to qualify several functionalities of the ROC, including tests with modules and system prototypes. The production of the next generation of RD53 chips (RD53B) [4] has started over the course of 2021, and its qualification will define the final version (RD53C) of the chips to be used by the experiments. The first prototype modules featuring the RD53B-CMS chip, also known as C-ROC, have been assembled in early 2022 as part of the development of the TEPX subdetector. This contribution presents the results of tests done on these first modules.

2 TEPX modules with RD53B-CMS readout chips

As in the current pixel detector, every module of the Phase-2 inner tracker features readout chips bump-bonded to a sensor and wire-bonded to a high-density interconnect (HDI). The latter is a flexible printed-circuit board (PCB) implementing the electrical connections needed to power and operate the modules. Different HDIs are used for the modules of the three subsystems (TBPX, TFPX, TEPX), mainly to accommodate for the different number of ROCs (two or four) present in a given module. These HDIs, while different, follow similar design choices. In the case of TEPX, all modules host four ROCs ("2×2 modules"), and feature the same HDI. The latter is designed to allow the use of different data-merging schemes, depending on the position of the module in the TEPX rings (more output links for modules in inner rings, fewer for modules in outer rings). The TEPX HDI for C-ROC modules has a size of $36 \times 44\,\mathrm{mm}^2$. A short pigtail, 25 mm-wide and 10 mm-long, provides the connections for power, high-voltage and signals. It matches a 50-pin connector on the TEPX disks. The HDI has three 18 µm-thick conductor layers of copper, and additional polyimide layers. Differential signal traces are impedance-matched to the readout link. The complete layer stack has a thickness of approximately 200 µm, and a mass of about 0.6 g including components. On the HDI's surface, fourteen pads are used to measure the module's input voltage, as well as the voltages of the digital and analog domains of the four ROCs. A picture of the first version of this HDI is given in figure 2 (left). Examples of different data-merging schemes implemented in this HDI are shown in figure 2 (right).

2023 JINST 18 C01027

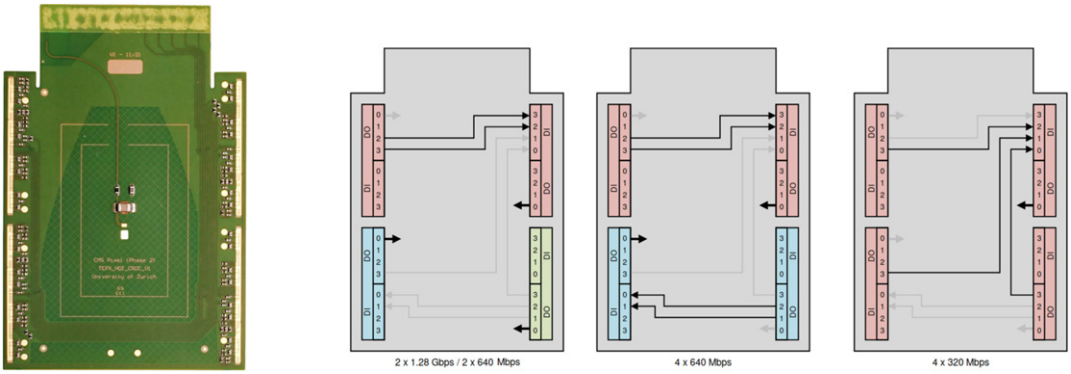

Figure 2. Left: picture of the first version of the TEPX HDI for 2 × 2 C-ROC modules (four ROCs per module); round pads for measuring the input, analog and digital voltages of the four ROCs can be seen close to three of the outer edges of the HDI. Right: examples of different data-merging schemes supported by this first version of the TEPX C-ROC HDI.

RD53B-CMS chips became available to module-production centers in early 2022, and soon after the first digital modules[1] were assembled. The first C-ROC digital modules were assembled at PSI in March 2022 for the TEPX subdetector. As of October 2022, C-ROC digital modules have been assembled for all three subsystems of the CMS Phase-2 inner tracker. In the following sections, results are shown for C-ROC digital modules of the TEPX subsystem.

2.1 Setup for module testing

A picture of the setup used to test the first TEPX C-ROC digital modules is shown in figure 3 (left). A dedicated PCB is used to connect the module to the power supply, as well as to the data-acquisition (DAQ) system. The latter is based on a FC7 board [5] which is connected to the module's PCB via a DisplayPort cable. The DAQ software and firmware used to operate the modules are developed by the Tracker group of the CMS Collaboration. During testing, a custom-made probe card equipped with needles, shown in figure 3 (left), is placed on top of the module. The needles are put in contact with the pads of the HDI in order to measure the input voltage on the module, as well as the regulated voltages of each of the four ROCs in their analog and digital domains. The modules are operated at constant input current; the typical input current used during tests is 8 A, corresponding to approximately 2 A per ROC. The backside of the module is in contact with a plate actively cooled to 18 °C. This allows maintaining the module's temperature at stable values, which are always kept below 35 °C during tests, based on measurements done with a thermal camera. This setup is a simplified prototype of the one that will be used during full-scale production. The final testing setup will feature a "cold box" capable of hosting up to eight modules, each connected to a probe card like the one in figure 3 (left). Peltier coolers will be used to test the modules at temperatures as low as −30 °C. A technical drawing of the final cold-box setup is shown in figure 3 (right).

[1] The term "digital module" denotes a module assembly without pixel sensors (only ROCs wire-bonded to a HDI).

2023 JINST 18 C01027

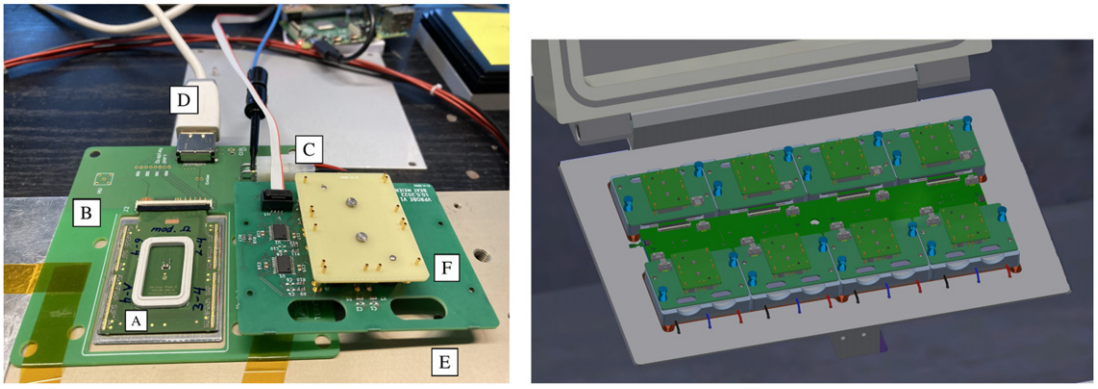

Figure 3. Left: picture of the setup used for the first tests on digital C-ROC modules for TEPX; a module (A) is mounted on a PCB (B) connecting it to the power supply (C) and DAQ system (D); the backside of the module is in contact with a plate (E) cooled to 18 °C; a probe card with needles (F) is placed on top of the module during testing to measure voltages from the pads on the surface of the HDI. Right: technical drawing of the cold-box setup to be used for module testing during full-scale production, hosting up to eight modules.

2.2 SLDO characterisation and tests of hit-data readout

Tests on these first digital modules included the characterisation of the ROCs' voltages as a function of input current of the module, as well as tests on the configuration of registers and readout of hit data induced via the charge-injection circuitry of the ROCs.

Figure 4 (top, left) shows the input voltage of the module, and the regulated analog and digital voltages of one of its ROCs, as measured by the probe card, as function of the input current of the module. In this example, the digital-to-analog converters (DACs) controlling the regulated voltages are tuned to give approximately 1.2 V for both. For a sufficiently high input current (above 7.5 A), the input voltage is in very good agreement with expectations (solid line), confirming the correct behaviour of the SLDO regulators. Figure 4 (top, right) shows measurements of a ROC's regulated voltages as function of the corresponding DACs, confirming that both voltages depend linearly on the DAC value. Figure 4 (bottom, left) shows the input current of each of the four ROCs of a module, as well as the current of its shunt regulators in the analog and digital domains, for an input current on the module of 9 A. These currents can be measured using the analog-to-digital converter (ADC) of the C-ROC's monitoring block. These measurements confirm that the current consumption is uniformly distributed across the four ROCs of the module, and the ADC values are properly calibrated (for example, the sum of the input currents of the four ROCs matches the module's input current of 9 A).

After the SLDO characterisation of the module, tests on the readout of hit data were carried out confirming the correct behaviour of the module. Figure 4 (bottom, right) shows a so-called "s-curve", the number of recorded hits divided by the number of injections as function of the injected charge in VCAL units (1 VCAL $\simeq$ 5.5 electrons) for all the pixels of one of the module's ROCs. As expected, all pixels reach full efficiency for sufficiently high injected charge; the average noise, obtained from fitting an error function to each of these turn-on curves, was around 90 electrons, which is compatible with the specifications of the read-out chip.

2023 JINST 18 C01027

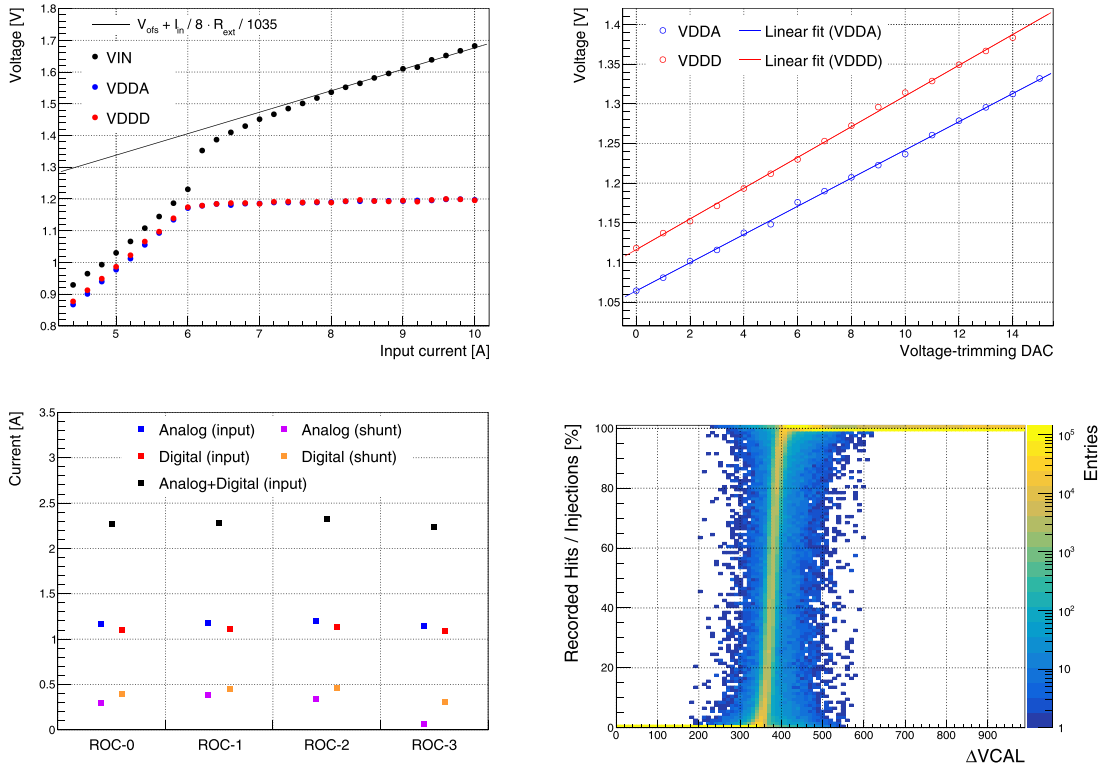

Figure 4. Top, left: module's input voltage (VIN), and regulated analog (VDDA) and digital (VDDD) voltages of one of the module's ROCs, as function of the module's input current. Top, right: VDDA and VDDD voltages of a ROC as function of the corresponding DACs. Bottom, left: input, analog-shunt current, and digital-shunt current of the four ROCs of a TEPX module, for an input current on the module of 9 A; these currents are measured using the ADC of the C-ROC's monitoring block. Bottom, right: number of recorded hits divided by the number of injections as function of the injected charge in VCAL units (1 VCAL $\simeq$ 5.5 electrons), also known as "s-curve", for all the pixels of one of the module's ROCs.

These tests on the first C-ROC modules yielded positive results. Tests on modules to verify the data-merging functionalities of the readout chip are in progress. Once modules with sensors will be assembled, tests on sensor bump-bonding quality and hit-efficiency measurements with particle sources (e.g. X-rays) will also be performed. The exact sequence of tests to be performed on each module during full-scale production is still under development.

3 Summary

This article presents the status of the assembly and testing of the first digital modules featuring the RD53B-CMS readout chip (also known as C-ROC), as part of the development of the CMS inner tracker for the HL-LHC. The results shown here focus on TEPX modules, each featuring four C-ROC chips and the first version of the TEPX C-ROC HDI. The results of the IV characterisation of these modules are in good agreement with expectations. These modules are found to work

2023 JINST 18 C01027

correctly while operating all of their four ROCs simultaneously: these first tests included the configuration of chip registers, the readback of monitoring information via the chip's ADC, the readout of hit data induced via charge injections, and the tuning of some of the main DACs controlling the response of each readout chip. Further tests on modules to verify the data-merging functionalities of the RD53B chip are in progress. C-ROC modules featuring pixel sensors will be assembled and tested in the near future. The results of these efforts will lead to the final design of the readout chip for the modules of the CMS Phase-2 inner tracker.

Acknowledgments

This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under the Marie Skłodowska-Curie Grant Agreement No. 884104 (PSI-FELLOW-III-3i).

References

[1] CMS Collaboration, *The CMS experiment at the CERN LHC,* 2008 *JINST* **3** S08004.

[2] CMS Collaboration, The Phase-2 Upgrade of the CMS Tracker, CERN-LHCC-2017-009, CMS-TDR-014 (2017), https://cds.cern.ch/record/2272264.

[3] RD53 collaboration, The RD53A Integrated Circuit, CERN-RD53-PUB-17-001 (2017), https://cds.cern.ch/record/2287593.

[4] RD53 collaboration, Introduction to RD53B Pixel Chip Architecture, Features, Performance and Recommendations for Use in Pixel Detector Systems, CERN-RD53-PUB-21-001 (2021), https://cds.cern.ch/record/2754251.

[5] M. Pesaresi et al., *The FC7 AMC for generic DAQ & control applications in CMS,* 2015 *JINST* **10** C03036.

2023 JINST 18 C01027