Computational Logic with Square Rings of Nanomagnets

Hanu Arava[1, 2], Peter. M. Derlet[3], Jaianth Vijayakumar[4], Jizhai Cui[1, 2], Nicholas. S. Bingham[1, 2], Armin Kleibert[4] and Laura. J. Heyderman[1, 2]

[1]Laboratory for Mesoscopic Systems, Department of Materials, ETH Zurich, 8093 Zurich, Switzerland

[2]Laboratory for Multiscale Materials Experiments, Paul Scherrer Institute, 5232 Villigen PSI, Switzerland

[3]Condensed Matter Theory Group, Paul Scherrer Institute, 5232 Villigen PSI, Switzerland

[4]Swiss Light Source, Paul Scherrer Institute, 5232 Villigen PSI, Switzerland

Scanning Electron Microscopy (SEM)

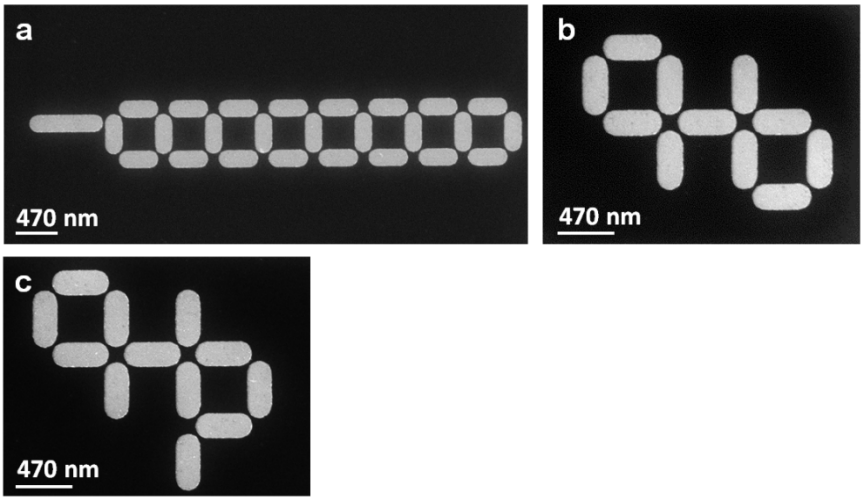

Figure S1. SEM images of (a) a square rings, (b) a pseudo-NAND logic gate and (c) a full NAND/NOR logic gate

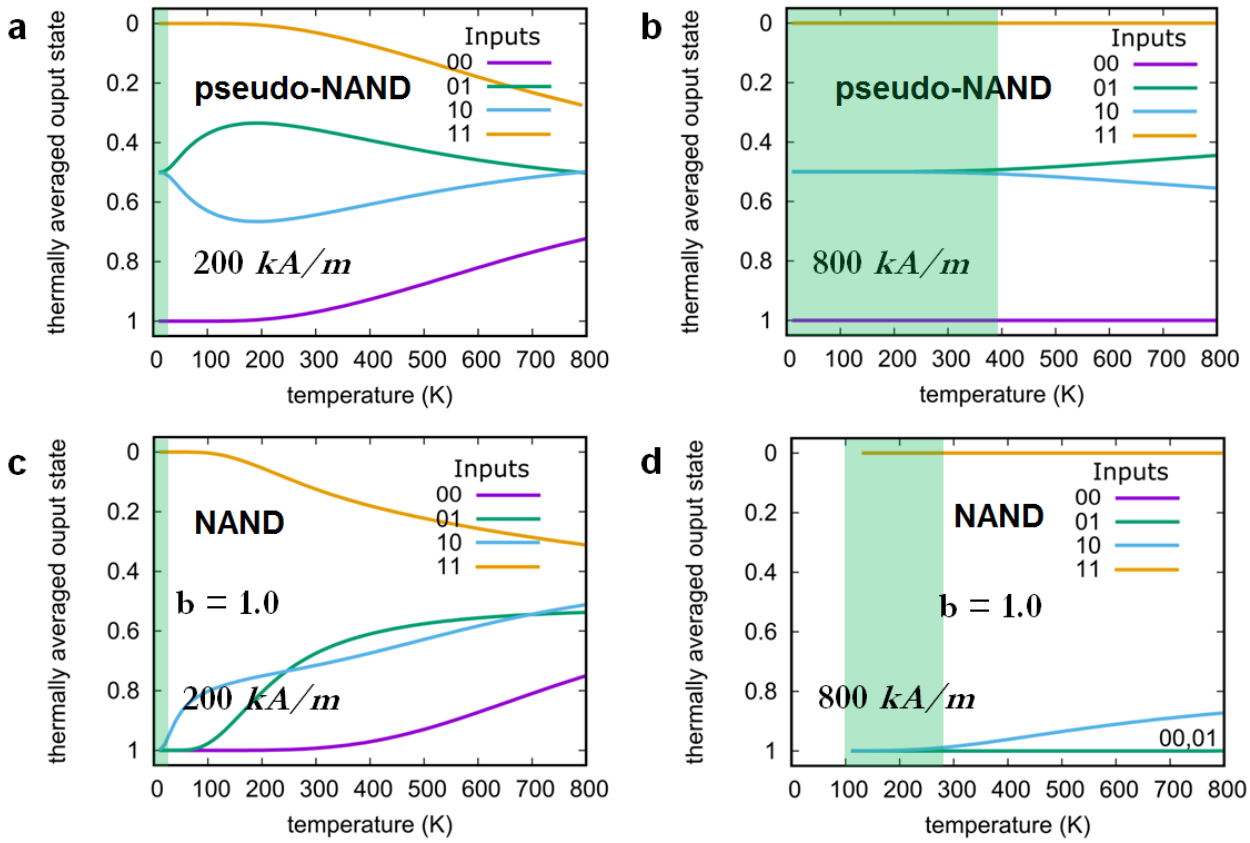

Figure S2. Simulated performance of pseudo-NAND and NAND gates as a function of temperature. Thermally averaged output state of (a, b) the experimentally measured pseudo-NAND gate and (c, d) the proposed NAND gate as a function of temperature for the four possible input states, (00), (01), (10) and (11), calculated for M_s = 200 kA/m and 800 kA/m. The green shaded region indicates the temperature range where the gates are expected to be fully reliable.

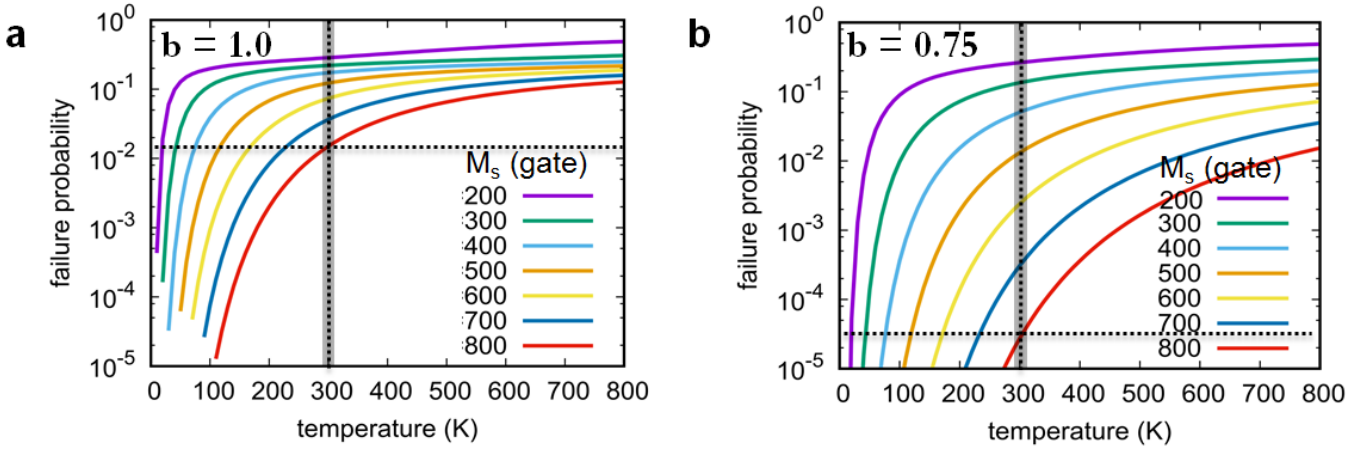

Figure S3. Plot of the failure probability as a function of temperature for the input state of (10) where the bias $\boldsymbol{b} = \frac{\boldsymbol{M_s(bias)}}{\boldsymbol{M_s(gate)}}$ is (a) 1.0 and (b) 0.75 for different values of the magnetization of all other nanomagnets in the gate. The grey bar in each plot indicates room temperature (~300 K) and the black dotted lines indicate the failure probability at room temperature for an M_s = 800 kA/m.

Full Gate Operations

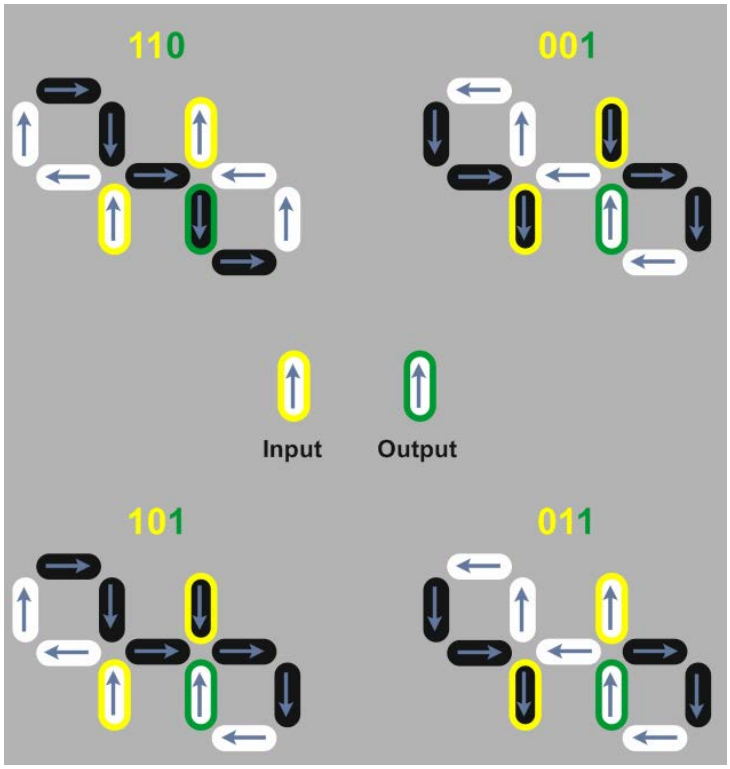

Figure S4. Logic performed with a pseudo-NAND gate. Schematically represented are the gate operations of (110), (001), (100) and (011), with inputs shown in yellow and the output in green. Gate operations (110) and (001) are energetically favourable. Operations involving (10) and (01) inputs have a ~50% probability of yielding the right output.

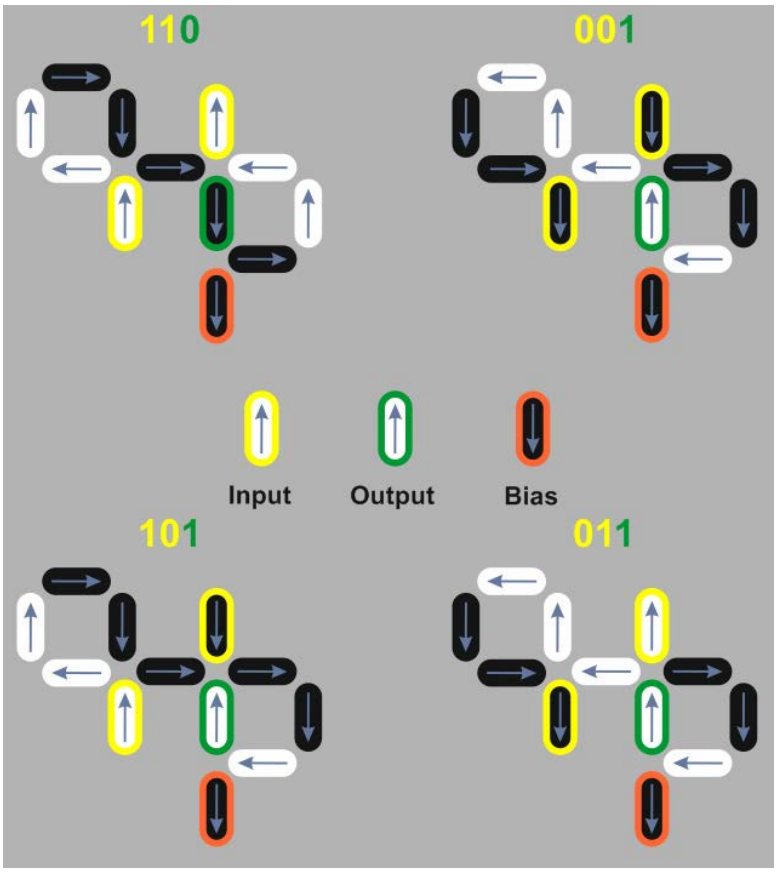

Figure S5. Logic performed with a NAND gate. Schematically represented are the gate operations of (110), (001), (101) and (011), with inputs shown in yellow, output in green and the bias in orange (which is always set with the moment down). All the operations are now energetically favourable and thus support a full NAND logic gate operation. With a reversed orientation of the magnetic moment of bias, the same design acts as a NOR gate.

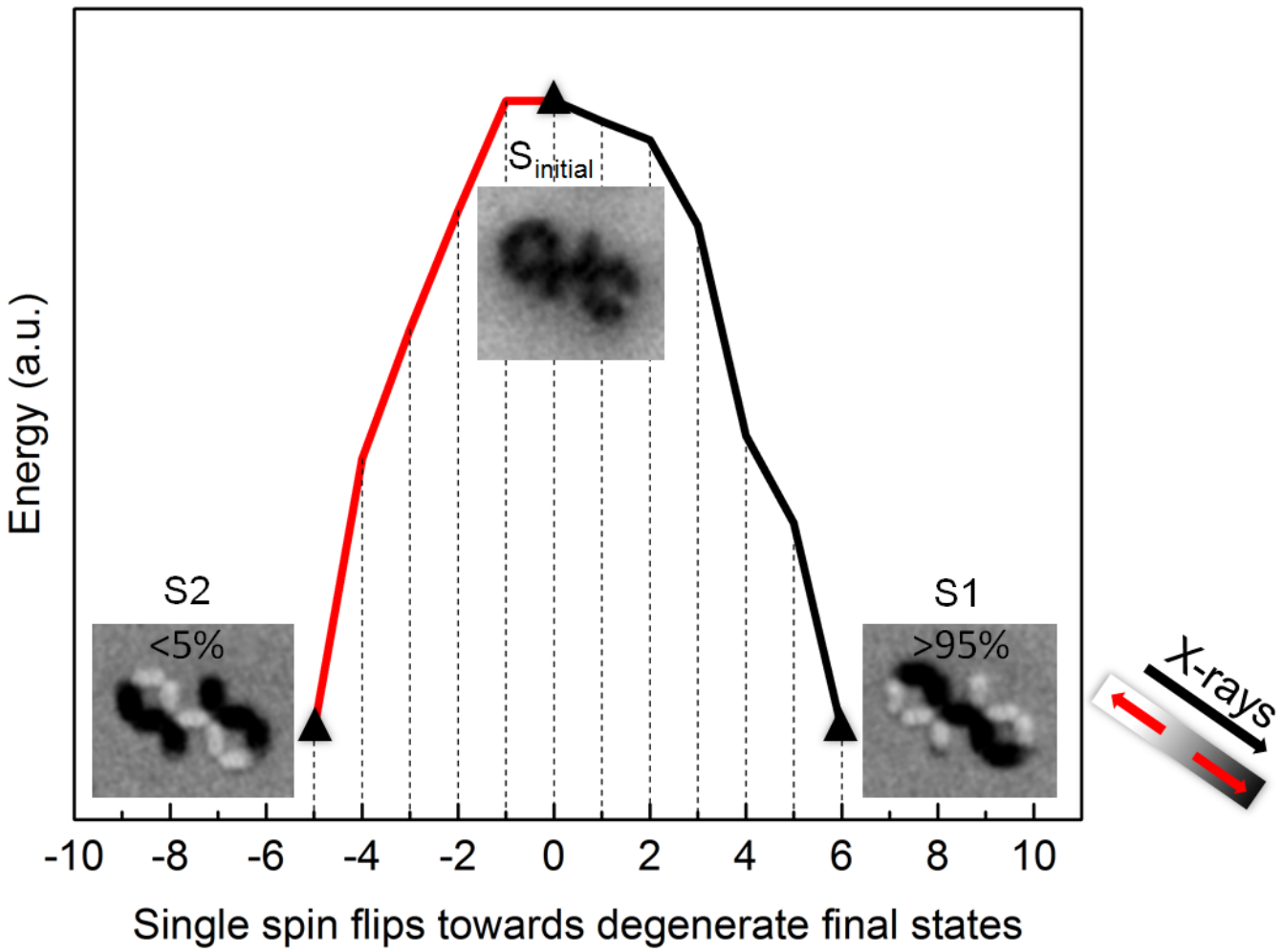

Figure S6. Preferred energy path for thermal relaxation of the pseudo-NAND gate. A pseudo-NAND gate in an initial spin configuration ($S_{initial}$), with all its moments pointing towards the direction of an initially applied field, thermally relaxes to one of two possible degenerate low energy states (S1 and S2). Via single spin flips, the gate passes through a number of configurations with a given energy. For the first spin flip, the first configuration on the path to S1 (in black) has a lower energy compared to the first configuration on the path to S2, and is therefore favoured. We observe that >95% of the pseudo-NAND gates end up in the degenerate state S1. This asymmetry in the probabilities occurs because the heating is terminated after a finite time.

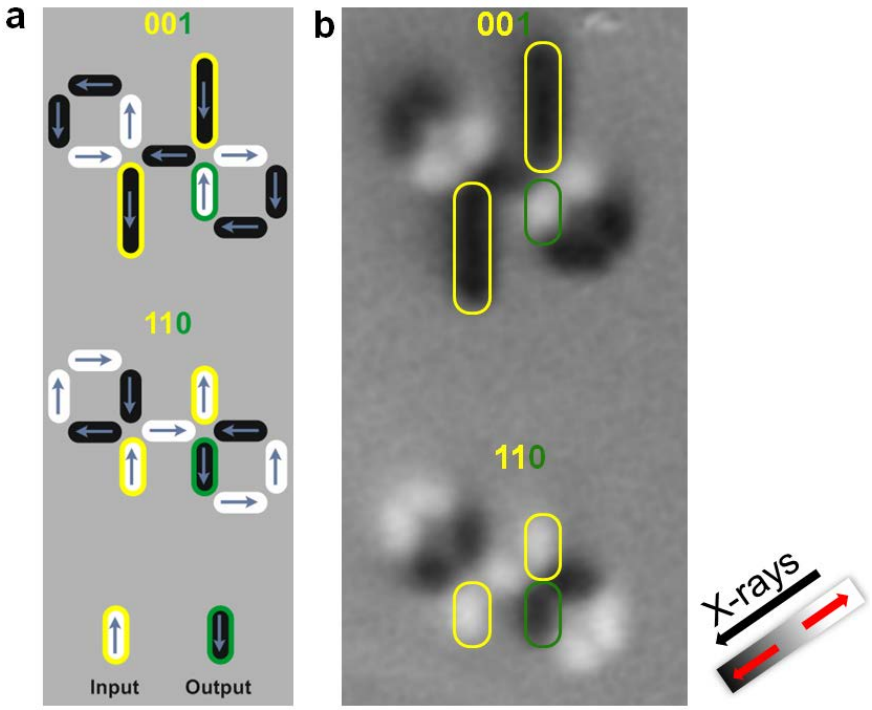

Figure S7. Two pseudo-NAND gates with long and short input nanomagnets. (a) Schematic and (b) X-PEEM images of the pseudo-NAND logic gates showing gate operations of (001) and (110) with long and short inputs, respectively. We observe successful operation of >90% gates for over 500 logic gates with long input nanomagnets. This demonstrates the possibility to control the operation of the gate.